Abstract

Fast multiplication is very important in processing of digital signals like DSP for convolution, Fourier Transform, etc. Many conventional methods are used for designing a multiplier for processing a digital signal. In this paper, A fast method for multiplication based on Ancient Indian Vedic mathematics is proposed. The whole of Vedic mathematics is based on 16 sutras (formulae). Among the various methods of multiplication in Vedicmathematics, Urdhava Tiryakbhyam (Vertically and Crosswise) is discussed in detail. This is the general multiplication formula applicable to all cases of multiplication. For implementation of a efficient Architecture simple Boolean logic is combined with Vedic formulas, which reduces the partial products and sums generated in one step. The coding is done in VHDL and synthesis is done using Xilinx ISE 9. 1i simulator. Results are compaired with several conventional techniques.

References

Implementation of an Efficient Multiplier Architecture over a Conventional Methods using Ancient Indian Vedic Sutra


**Index Terms**

Computer Science  
Artificial Intelligence

**Keywords**

Vedic mathematics  
Sutra  
Urdhava Tiryakbhyam  
VHDL.