Attempts are kept going to decrease energy consumption and reversible circuits are seen to be of high importance to do so. Reversible logic is used in some area such as Nanotechnology, quantum computing, optical computing and low-power CMOS design. In the present study a novel parity preserving reversible random access memory is designed. General designs for components of PPRRAM are introduced. In addition a new reversible gate, PH3, is introduced which is Parity preserve and capable of being utilized in various reversible circuits. We have used it to design parity preserving reversible master slave D flip-flop and parity preserving memory cell. The proposed master slave D flip-flop and write enable master slave D flip-flop is compared with existing works and its efficiency is shown in terms of gate counts and garbage outputs. All the scales are in the Nano metric area.
Theoretical Physics, 21: 219-253.


Index Terms

Computer Science

Integrated Circuits
Keywords

Reversible Logic  Parity Preserving  Random Access Memory  Flip-flop  Garbage

Output