Analysis of GDI Technique for Digital Circuit Design

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Abstract

Power Dissipation of Digital circuits can be reduced by 15% - 25% by using appropriate logic restructuring and also it can be reduced by 40% - 60% by lowering switching activity. Here, Gate Diffusion Input Technique which is based on a Shannon expansion is analyzed for minimizing the power consumption and delay of static digital circuits. This technique as compare to other currently used logic design style, allows less power consumption and reduced propagation delay for low-power design of combinatorial digital circuits with minimum number of transistors. In this paper, basic building blocks of digital system and few combinational circuits are analyzed using GDI and other CMOS techniques. All circuits are designed at 180nm technology in CADENCE and simulate using VIRTUOSO SPECTRE simulator at 100 MHz frequency. Comparative analysis has been done among GDI and other parallel design styles for designing ripple adder, CLA adder and bit magnitude comparator. Simulation result shows GDI technique saves 53. 3%, 55. 6% and 75. 6% power in ripple adder, CLA adder and bit magnitude comparator respectively as compare to CMOS. Also delay is reduced with 25. 2%, 3. 4% and 6. 9% as compare to CMOS. Analysis conclude that GDI is revolutionary high speed and low power consumption technique.
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References

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Index Terms
Keywords
CMOS  GDI  SOI  CLA.