Abstract

This paper presents an efficient Low-Power Viterbi Decoder Design using T-algorithm. It implements the viterbi decoder using T-algorithm for decoding a bit-stream encoded by a corresponding forward error correction convolutional encoding system. A lot of digital communication systems incorporated a viterbi decoder for decoding convolutionally encoded data. The viterbi decoder is able to correct errors in received data caused by channel noise. We proposed an architecture implementing a Viterbi Decoder with T-algorithm deployed with threshold generator unit and purge unit to reduce the number of states which reduce power consumption. We propose modified architecture for the survivor Metric Unit to reduce the memory Access power during the trace back operation. The proposed viterbi decoder is carried out for rate-1/2 with a standard constraint length 7. The Synthesis results will be done using cadence RTL Encounter Tool. For ASIC synthesis, we use TSMC 45-nm CMOS Process. The architecture which reduces the complexity and power Consumption by as much as 70% without effecting the decoding speed.
References

- "Bandwidth-efficient modulations," Consultative Committee For Space Data System, Matera, Italy, CCSDS 401(3. 3. 6) Green Book, Issue 1, Apr. 2003.

Index Terms

Computer Science

Algorithms

Keywords

Viterbi Decoder (VD) Convolutional Code Constraint Length Code rate VLSI Trellis Diagram