Abstract

In Wireless communication is one among the foremost vivacious analysis areas within the communication field these days. This paper presents the implementation of FSM based WLAN and modified FSM based WiMAX interleaver in VHDL. For WLAN the implemented interleaver is compared with the available works. A modification in the FSM of address generator for WiMAX interleaver provides a significant 35.8% enhancement in terms of logic cells and 22% enhancement in terms of slice flip flops used, as compared to available work [41]. The circuit parameters and simulation results obtained using ModelSim XE II software are also presented.

References

- Konhauser, W., 2006, Broadband wireless access solutions progressive challenges and potential value of next generation mobile networks, International Conference on Wireless
An Amendment to FSM based Interleaver for WLAN and WiMAX in VHDL

- Altera Inc. , Symbol Interleaver/De-Interleaver Core, Mega core function user&apo;s guide, ver. 1. 3. 0, June 2002.
- Tell, E. and Liu, D. , 2004, a hardware architecture for a multimode block interleaver, ICCSC, Moscow, Russia, June 2004.
- Asghar, R. and Liu, D. , 2009. Low complexity multimode interleaver core for WiMAX
An Amendment to FSM based Interleaver for WLAN and WiMAX in VHDL


Index Terms

Computer Science Wireless

Keywords

WLAN FSM WiMAX VHDL Xilinx ModelSim.