Abstract

In this paper an effort is made to design a stable and energy efficient asymmetrical 6T SRAM cell in 65nm technology generation with one bit line for read and one for write operation along with dual word lines. A simple energy recovery driver is added to enhance the write ability of the SRAM and to recover energy. Sizing the access transistor helps write ability and sizing of the pull down transistor provides better read stability. This circuit saves energy during write operation and also provides good read stability.

References

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- PTM models derived from http://ptm.asu.edu/

Index Terms

Computer Science

Circuits And Systems
Keywords
- SRAM
- energy
- stability
- bit line