Abstract

A parallel-prefix adder gives the best performance in VLSI design. However, performance of Ladner-Fischer adder through black cell takes huge memory. So, gray cell can be replaced instead of black cell which gives the Efficiency in Ladner-Fischer Adder. The proposed system consists of three stages of operations they are pre-processing stage, carry generation stage, post-processing stage. The pre-processing stage focuses on propagate and generate, carry generation stage focuses on carry generation and post-processing stage focuses on final result. In ripple carry adder each bit of addition operation is waited for the previous bit addition operation. In efficient Ladner - Fischer adder, addition operation does not wait for previous bit addition operation and modification is done at gate level to improve the speed and to decreases the memory used.

References

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Design of Efficient 16-Bit Parallel Prefix Ladner-Fischer Adder


Index Terms
Computer Science
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Keywords
Ripple carry adder  Efficient Ladner–Fischer adder  Black cell  Gray cell