Abstract

In this paper, a low power implicit type pulsed flip-flop (PFF) using self-driven pass transistor logic is presented. The pulse generation logic comprising of two transistor AND gate is used in the critical path of the design for improved speed and reduced complexity. The pass transistor logic driven by generated clock pulse is used directly to drive the output of the flip-flop. The proposed design is compared with the conventional implicit type data close to output (ip-DCO) flip-flop. As compared to the conventional pulse triggered flip-flop, the proposed pulsed flip-flop (PFF) design features best speed, power and power-delay-product performance. The proposed technique is implemented using HSPICE CMOS 90nm technology. The average power consumption for 50% switching activity is reduced by 12.75% as compared to conventional ip-DCO.

References

Low Power Pulsed Flip-Flop using Self Driven Pass Transistor Logic


Index Terms

Computer Science Integrated Circuits

Keywords

Low power pulsed flip-flop pass transistor logic critical path power-delay-product