Abstract

In this paper, an energy efficient design of asymmetric high performance low swing CMOS driver receiver pair for driving global on-chip interconnects is proposed. The design is implemented on 90nm CMOS technology using HSPICE. The proposed CMOS driver receiver pair reduces the power by 35.45% as compared to the static driver with conventional level converter (CLC). The design is also compared with the asymmetric source follower driver with level converter (ASDLC), which results in high performance and low power consumption with reduced circuit complexity.

**Index Terms**

Computer Science  
Digital Circuits

**Keywords**  
Low swing  
CMOS driver receiver pair  
level converter  
asymmetric source follower  
driver  
global on-chip  
interconnects.