Abstract

Main constraint for any VLSI system is power, speed and area but power consumption is major hurdle for system performance. In this paper a series of improved power efficient sequential elements (flip-flops) are presented. Such as conditional data mapping flip-flop (CDMFF), clocked pair shared flip-flop (CPSFF) and new proposed flip-flop in which dual edge triggered technique is used. In conditional data mapping methodology the less power consumption achieved by mapping the inputs in such way that eliminates the unnecessary transitions. But CPSFF the clock load is minimized it leads to power saving. In new propose technique clock frequency could reduce by half then the power dissipation due to clock transitions can be reduced by half it leads to power efficient model flip-flop.

References


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delay and energy of single edge-triggered & dual edge-triggered pulsed ?ip-?ops for high performance microprocessors,&quot; in Proc. ISPLED, Huntington Beach,CA,Aug. 2001,pp. 207–212

Index Terms
Computer Science
 Applied Sciences

Keywords
Data mapping   Clock load   CPSFF   Flip-flop   Power   Edge- triggered