Abstract

Demand of low power circuits design is increasing due to the large growth in portable digital equipment. In this reference adiabatic structure are used that provides a dramatic reduction in power dissipation by recycling some of the energy from output load capacitor and saving power in upper half of the network instead of dissipated as heat. In this paper a low power multiplexer based 4-2 compressor is designed using Positive feedback adiabatic logic. The compressor design is simulated at 0.12µm technology using Microwind 3.1. Simulated results shows that proposed design saves 54.9% power than conventional CMOS based compressor.

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Index Terms

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BSIM CMOS VLSI PFAL Multiplexer.