Abstract

With the advancement of Network-on-chip (NoC), fast and fair arbiter as the basic building block for high speed switches/routers gained attention in recent years. In this paper I propose the fair chance round robin arbiter (FCRRA), a high speed, low power and area efficient RRA for NoC applications. The FCRRAG tool propose in this paper can generate a design for bus arbiter, which can handle the exact number of bus masters for both on chip and off chip buses within one short cycle.

References

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