Abstract

The two different architectures for adders are introduced in this paper. The first one is built around a sparse carry computation unit that computes only some of the carries of modulo 2n+1 addition. This sparse approach is enabled by the introduction of inverted circular idem potency property of the parallel-prefix carry operator and its regularity and area efficiency are further enhanced by the introduction of a new prefix operator. The resulting diminished-1 adder can be implemented in a smaller area and consume less power compared to all earlier proposals, maintaining a high operation speed. The second adder architecture unifies the design of modulo 2n+1 adder. Both the adders are derived and compared by using the simulation results.

References

Design of High Speed Modulo 2n+1 Adder

- K. Nehru, A. Shanmugam and S. Vadivel, "Design of 64-Bit Low Power Parallel Prefix VLSI Adder for High Speed Arithmetic Circuits."
Design of High Speed Modulo 2n+1 Adder

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