Abstract

Aggressive Packet Combining (APC) scheme is well established in literature for receiving correct packet in high error prone wireless link. Several modifications were earlier studied elsewhere for improving throughput and decreasing latency. In APC three copies of a packet are transmitted and receiver does bit wise majority decision to get correct copy. Main research challenge of the APC is if two or more copies of the packet become erroneous at a particular bit location(s) the operation of the majority logic fails to correct the error. To address the above drawback of the APC, three new modifications of APC are proposed in this paper. The proposed techniques are found to provide better throughput & high error correction probability.
Three New Investigations of Aggressive Packet Combining to Get High Throughput

References

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Index Terms

Computer Science Circuits And Systems
Keywords
Packet Combining Scheme  Conventional Aggressive Packet Combining Scheme (CAPC)  Throughput  Bit error rate  three paths  XOR  half bit exchange.