Abstract

In this paper an area efficient 17T 1-bit hybrid comparator design has been presented by hybridizing PTL and GDI techniques. The proposed 1-bit comparator design consist of 9 NMOS and 8 PMOS. A PTL and GDI full adder module has been used which consume less area at 120 nm as compared with the previous full adder designs. The proposed Hybrid 1-bit comparator design is based on this area efficient 9T full adder module. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the used full adder module. Full adder modules outputs have been used for the generation of three different output of 1-bit comparator designs. The proposed 1-bit comparator has been designed and simulated using DSCH 3. 1 and Microwind 3. 1 on 120nm. Also the simulation of layout and parametric analysis has been done for the proposed 1-bit comparator design. Power and current variation with respect to the supply voltage has been performed on BSIM-4 and LEVEL-3 on 120nm. Results show that area consumed by the proposed hybrid adder is 329.3µm² on 120nm technology. At 1. 4V input supply voltage the proposed 1-bit hybrid comparator consume 0. 367mW power at BSIM-4 and 0. 411mW power at LEVEL-3 and 2. 313mA current at BSIM-4 and 3. 047mA current at LEVEL-3 model.
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**Index Terms**

Computer Science Digital Circuits

**Keywords**

BSIM CMOS Gate Diffusion Input NMOS PMOS Pass transistor logic VLSI