Abstract

This paper presents the application of geometric programming for combined high-level and low-level architecture parameter exploration. This paper builds an geometric programming framework for reconfigurable architectures, and presents a full delay and area model of an FPGA. This optimization allows high-level architectural parameter selection and the transistor sizing to be done concurrently. The transistor values are derived using 45nm predictive technology model. CVX framework for MATLAB is used to run the geometric programming framework. The area and critical path delay are determined for given cost function by single-stage and multi-stage approach.

References

Area-Delay Estimation by Concurrent Optimization of FPGA Architecture Parameters using Geometric Programming


Index Terms

Computer Science

Digital Circuits
Keywords
- Geometric Programming
- Reconfigurable architectures