Abstract

As transistor sizes scale down and levels of integration increase, leakage power has become a vital downside in modern low-power VLSI technology. This is often very true for ultra-low-voltage (ULV) circuits, wherever high levels of leakage force designers to selected relatively high threshold voltages, which limits performance. In this paper, we design different design approach of master slave D flip-flop with stacking power gating leakage reduction technique. Here these techniques essentially increase the effective resistance of leakage paths by adding sleep transistors between logic stacks and power supply rails. Power gating technique also provides many of the property from transistor stacking technique. The proposed approach saves maximum amount of the Leakage power without degrading the performance of the circuit. In this work we analyses the leakage power of three different types of CMOS design style such as pass transistor logic (PTL), transmission gates and gate diffusion input (GDI) design. All these proposed circuits are simulated with and without the application of leakage reduction techniques. The circuits are simulated using Cadence Virtuoso tool at 45nm technology for various parameters.
References

Reduction of Leakage Power using Stacking Power Gating Technique in Different CMOS Design Style at 45Nanometer Regime


Index Terms

Computer Science

Circuits And Systems

Keywords

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(GDI)
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