Abstract

Multi Valued Logic [MVL] is emerging as a promising choice for future computing technology. MVL has seen major advancement in the recent past due to several advantages offered by them over the binary logic, thus making it a thrust area for further research. The instruction set of the processor is its inherent entity. This paper presents design and implementation of an efficient instruction set for a ternary processor using Very-High-Speed Integrated Circuits, VHSIC Hardware Description Language [VHDL]. Twenty one instructions including various addressing modes such as register, direct and immediate mode are designed and implemented for 4-trit ternary processor. The required control signals are appropriately identified in the proposed design and enable the smooth operation of instructions. The designed 4 – trit instruction set signifies encouraging results that will pave the path for further developments in ternary processors.
- Sheng, L., Yong-Bin, K., Fabrizio, L.: CNTFET- based design of ternary logic gates and arithmetic circuits, IEEE transactions on nanotechnology, 10(2), March 2011.

Index Terms

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Keywords
Multi Valued Logic  Ternary logic  VHDL.