Abstract

As technology has scaled down, the implications of leakage current and power analysis for memory design have increased. To minimize the short channel effect Double-gate FinFET can be used in place of conventional MOSFET circuits due to the self-alignment of the two gates. Design for XOR and XNOR circuits is suggested to improve the speed and power. These circuits act as basic building blocks for many arithmetic circuits. This paper contrasts and evaluates the performance of conventional CMOS and FinFET based XOR-XNOR circuit design. It is based on the study of high speed, low power, and small area in XOR-XNOR digital circuits. The proposed FinFET based XOR and XNOR circuits have been designed using Cadence VIRTUOSO Tool applying voltage supply of 0.2 to 1.2 voltages, with temperature at 270°C and all the simulation results have been generated by Cadence SPECTRE simulator at 45nm technology. Simulation results exhibit low power, delay, power, delay product (PDP), and average dynamic power consumption.
Analysis of Conventional CMOS and FinFET based 6-T XOR-XNOR Circuit at 45nm Technology

- Seid Hadi Rasouli, Hanpei Koike, Kaustav Banerjee, "High-Speed Low-Power FinFET Based Domino Logic.&quot; Design automation conference 978-1-4244-2749-9/09, pp. 829-834.
- Jakub Kedzierski, Member, Meikei Ieong, Thomas Kanarsky, Ying Zhang, and H. -S. Philip Wong, "Fabrication of Metal Gated FinFETs Through Complete Gate Silicidation With Ni"; IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 51, NO. 12, DECEMBER 2004, pp. 2115-2120.
Applications (ICEDSA).


**Index Terms**

Computer Science  
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**Keywords**

XOR-XNOR gate; low power; delay; PDP.