Abstract

Today, in the world of ASICs and system-on-chip (SoC) designs which consists of millions of
transistors and gates, verification is the process which consumes most of design efforts and
time [4]. One of the major stresses for the verification engineer is to verify the given design in
best possible manner [5]. For this he needs to cover almost all the hidden corners cases by
applying various real time test cases. This paper will assist the verification engineers to
understand the flow of verification environment for packet switch IP. We will also learn about
the functional coverage. The language used for verification is SystemVerilog.

References

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Index Terms

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Keywords

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