Abstract

Network on Chip (NoC) has emerged as a viable solution to the complex communication requirements of constantly evolving System on Chip (SoC). The communication centric architecture of NoC can be optimized across a variety of parameters as per the design requirements. With the development of customized application the inclination has shifted from regular architectures to irregular topology which leaves researchers with larger spectrum of optimization parameters. Many heuristic methods have been explored as the optimization problems encountered are NP-hard. This paper presents a customized topology generator STG-NoC which implements a heuristic technique based on simulated annealing for achieving the objective of energy optimization.

References

- Busetti, F. 2003. Simulated annealing overview. citeseerx. ist. psu. edu

Index Terms

Computer Science
Communications
**Keywords**

Customized Network-on-Chip (NoC)  Energy optimization  Simulated Annealing  STG-NoC

(Simulated Annealing based Topology Generator for Network on Chip).