Abstract

Multiplier is the most basic unit of any electronic hardware whether it is microprocessor in cell phone or any DSP's processors for signal processing. So power dissipation by multiplier is the most important parameter which is needed to be taken care of. So a lot of researches have been made till now and lot of efforts has been made to decrease the power consumption of this basic unit. From last few years number of promising technologies came into existence which had opted by electronic industries to reduce the power consumption of whole system so the battery backup can be increased and less energy will be wasted for different computations. The most dominant technology in VLSI till now is cmos. The static power dissipation is due to leakage current and the dynamic power dissipation is due to switching transient current as well as charging and discharging of load capacitance. Power of any multiplier can be reduced by simply designing a full adder which will consumes very less power [8]. Number of techniques arrives in past researches to reduce the power consumption of multipliers. Reversible computing gives new direction to low power VLSI and important Reversible gates are mentioned in this paper. Various different architecture of multiplier using reversible gates for reducing power is discussed.
Architectures and Methodologies for Reducing Power in Multipliers: A Literature Survey

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