Abstract

In the modern era of electronics and communication decoding and encoding of any data(s) using VLSI technology requires low power, less area and high speed constrains. The viterbi decoder using survivor path with necessary parameters for wireless communication is an attempt to reduce the power and cost and at the same time increase the speed compared to normal decoder. This paper presents three objectives. Firstly, an orthodox viterbi decoder is designed and simulated. For faster process application, the Gate Diffused Input Logic (GDIL) based viterbi decoder is designed using Xilinx ISE, simulated and synthesized successfully. The new proposed GDIL viterbi provides very less path delay with low power simulation results. Secondly, the GDIL viterbi is again compared with our proposed technique, which comprises a Survivor Path Unit (SPU) implements a trace back method with DRAM. This proposed approach of incorporating DRAM stores the path information in a manner which allows fast read access without requiring physical partitioning of the DRAM. This leads to a comprehensive gain in speed with low power effects. Thirdly, all the viterbi decoders are compared, simulated, synthesized and the proposed approach shows the best simulation and synthesize results for low power and high speed application in VLSI design. The Add-Compare-Select (ACS) and Trace Back (TB) units and its sub circuits of the decoder(s) have been operated in deep pipelined manner to achieve high transmission rate. Although the register exchange based
survivor unit has better throughput when compared to trace back unit, but in this paper by introducing the RAM cell between the ACS array and output register bank, a significant amount of reduction in path delay has been observed. All the designing of viterbi is done using Xilinx ISE 12.4 and synthesized successfully in the FPGA Virtex 4 target device operated at 64.516 MHz clock frequency, reduces almost 41% of total path delay.

References

- www.xilinx.com/training/languages/designing-with-vhdl.htm
- www.digilentinc.com/Products/Detail.cfm?NavPath=ATLYS
Index Terms

Computer Science
Circuits And Systems

Keywords
Viterbi decoder  GDIL technique  SPU  DRAM  Add Compare Select (ASC)
Trace Back (TB)

Xilinx

FPGA.