Abstract

Dynamic CMOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. These circuits require less number of transistors as compare to CMOS logic circuits. But they suffer from limitations such as noise tolerance, charge leakage, and power consumption. This noise induce in circuits will affect the performance of dynamic circuits. The our work base on noise of MOSFET in contrast to the conventional method which measures drain current noise of MOSFET and divides it by MOSFET transconductance. Therefore, the need for accurate measurement of I–V characteristics of the MOSFET is eliminated, leading to the better accuracy of the measured noise. To design a noise tolerable circuit using dynamic CMOS logic, a new noise tolerant technique is proposed here and then with the help of software we perform parametric analysis to improve the parameters such as noise margin, worst case delay, delay uncertainty, delay sensitivity from their initial performances. By studying those effects we try to put such parameters which help us to make a noise tolerable circuit.
References


Index Terms

Computer Science          Circuits And Systems

Keywords

Dynamic Logic Structure    Charge sharing    Keeper logic