Low Power 3T XOR Cell using IDDG MOSFET

Abstract

In this paper, a new design of three transistor XOR gate is proposed using Independent Driven Double Gate MOSFET to achieve ultra-low power in sub threshold conduction. The proposed design has been compared with the three transistor XOR implemented using Symmetrical Driven Double Gate MOSFET in sub threshold region. A three transistor XOR gate designed using Independent Driven Double Gate MOSFET is showing improved results in terms of power consumption with varying input voltage, temperature and operating frequencies. The simulation has been carried out on SPICE tool at 45 nm technology.

References


Index Terms

Computer Science Circuits And Systems

Keywords

DG MOSFET low power sub threshold XOR gate.