Design of Pulse Detectors and Unsigned Sequential Multiplier using Reversible Logic

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Abstract

International Technology Roadmap for Semiconductors (ITRS) set a road map for More than Moore (MtM). Where device is scaled more than what the moore's law predicts. This MtM scaling will leads to substantially large design in the future and also huge power dissipation due to irreversible logic computation. Since applying low power technique has become tedious and time consuming. The solution is reversible logic computation. It plays an important role in power dissipation reduction. A novel design of reversible pulse detectors and sequential multiplier are proposed in this paper. As far as it is known, this is the first attempt to apply reversible logic to Pulse detectors and sequential multiplier. This paper also proposed a new reversible gate which can be used as full adder or full subtractor.

References


**Index Terms**

- Computer Science
- Circuits And Systems
Keywords
Low power VLSI  Reversible logic  Reversible pulse detectors  Reversible full adder or full subtractor

Reversible sequential multiplier.