Abstract

A VLSI architecture of Syndrome generator is part of well known Reed Solomon codes which is capable of generating syndromes while receiving RS (N, K) Codes from the transmitter. RS codes are customized to achieve a suitable VLSI realization of syndromes which can be further used in error detecting algorithms such as Euclidean, Erasures, Berlekamp's iterative algorithm and Massey Linear feedback shift register synthesis algorithm. It is assumed to be one of the pipelining stages in the Reed Solomon decoding technique. A MATLAB implementation of syndrome generator with various RS codes having different ranges of bit symbols and codeword was reveal for the purpose of determining syndromes. Hardware intricacy depends only on 2p parity check bytes. Message is encoded in Galois field having $2^m$ elements. Each Codeword enclose symbols; symbol generates syndromes for those symbols. It represented implementation of RS (128, Kx) and RS (64, Ky) with the different values of bits/symbol and different range of Kx & Ky and look into how limit of Zeros and Syndrome varies.
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**Index Terms**

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**Keywords**

Syndromes Reed Solomon decoders pipelining processing Galois field VLSI error detection generator polynomial.