Abstract

This paper presents an efficient explicit pulsed static dual edge triggered flip flop with an improved performance. The proposed design overcomes the drawbacks of the dynamic logic family and uses explicit clock pulse generator approach to achieve dual edge triggering. The proposed flip-flop is compared with existing explicit pulsed dual edge triggered flip-flops. Based on the simulation results overall improvements of 12.67% and 10.15% are observed in delay and power delay product respectively.

References

A High Speed Explicit Pulsed Dual Edge Triggered D Flip Flop

Mar. 1996.


**Index Terms**

Computer Science  
Circuits And Systems

**Keywords**

Power delay product  
flip flop  
power consumption  
propagation delay  
CMOS  
logic  
transmission gate  
explicit pulsed.