Abstract

This paper presents a new low power 2-Bit magnitude comparator using full adder technique. The proposed magnitude comparator (PTL logic) has been compared with existing magnitude comparator (GDI technique). The performance analysis of both magnitude comparators is done on basis of power consumption with respect to input voltage, temperature, and frequency; using Tanner EDA tool version 12.6 at 45nm technology. The simulation results of proposed magnitude have shown remarkable performance in terms of power consumption, area and threshold loss in comparison to existing magnitude comparator. Thus proposed magnitude comparator can be viable option for low power application.

References


**Index Terms**

Computer Science  
Circuits And Systems

**Keywords**

Magnitude comparator  
PTL logic  
GDI technique  
full adder and Low power.