Abstract

Rapidly increasing design complexity due to small size and higher speed, results in the problem of clock skew and insertion delay. These are the two important parameters which should be considered for successful completion of the design. In this work, a method for minimizing clock skew by buffer insertion and resize is proposed. Clock skew will be minimized during post-CTS timing analysis after placement of standard cells during physical implementation of the design. Also, buffer relocation method is used for minimizing the delay of the cells. Simulations were carried out on EDA tools and results show that overall skew is improved by 23.95% and delay is improved by 19.50%.
Minimizing Skew and Delay with Buffer Resizing and Relocation during Clock Tree Synthesis

- Baris Taskin and Ivan S. Kourtev, "Performance optimization of single-phase level-sensitive circuits using time borrowing and non-zero clock skew," in proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of


- Video Tutorial Place and Route with Cadence SOC Encounter (Basics) available on URL: http://www.youtube.com/watch?v=Z5WKIDbthdg.


**Index Terms**

Computer Science

Algorithms
Keywords
Buffer  CTS  Delay  Skew  Slack.