Abstract

In this proposed design it mainly includes USB 3. 0, Physical Layer along with USB 2. 0 functionality with Super speed functionality. Physical Layer mainly contains PCI Express and PIPE interface. This proposed design transferred data from transmitter to receiver serially. This design manages to transfer data either on 2. 5GT/s or on 5. 0GT/s depends upon the mode and rate. The design generates clock that runs on two different frequencies i.e. 125MHz and 250MHz that used to transfer data on parallel interface. This Design manages to capture the data that are coming asynchronously and lock the receiver clock with incoming asynchronous serial data. The architecture for USB 3. 0 Physical Layer has been proposed in this paper. The
Implementation of USB 3.0 SuperSpeed Physical Layer using Verilog HDL

The proposed model is implemented and verified using Verilog HDL.

References

- "Lattice Semiconductor Corporation 8b/10b Encoder/Decoder", February 2012.

Index Terms

Computer Science
Circuits And Systems

Keywords