Abstract

The use of Vedic mathematics lies in the fact that it reduces the typical calculation in the conventional mathematics to very simple once. This is so because the Vedic formulae have claimed to be building on the natural principles on which the human mind works. Vedic mathematics is a several effective algorithms, which has spread over to various branches of engineering such as computing. In computers, typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operation. In this work, I have studied different multipliers, which give low power requirement and high speed, also give information of "urdhva-Tiryabhyam" algorithm of ancient Indian Vedic mathematics, which has utilized for multiplication to improve speed of multipliers. The proposed algorithm has modeled using VHDL, a hardware descriptive language. In a work I have simulated and synthesized 32-bit multiplier, the result shows that multiplier implemented using Vedic multiplication is efficient in terms of speed.

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**Index Terms**

- Computer Science
- Circuits And Systems
Keywords

Vedic Mathematics  Multiplier  Urdhva-Tiryabhyam