Abstract

As the utilization of multiprocessors system-on-chip (MPSoC) is becoming ubiquitous, demands for effective allocation and scheduling techniques are needed more than ever to harness the power of MPSoCs. An MPSoC is a system consisting of multiple heterogeneous processing cores, memory hierarchies, and communication infrastructure to effectively overcome the power and clock constraints from single core architectures. MPSoCs provide the performance demanded by embedded applications especially real-time multimedia applications. This article presents effective techniques to partitioning the processing cores and memory budget in an MPSoC among multiple embedded applications possibly entering the system at different times. The proposed framework will study the structure of each application and predict the possible reduction in schedule time if more processors and/or memory budget are assigned to this application. The objective is to fairly divide the resources such that the schedule times for the applications are minimized. Results on different embedded applications workloads and under different system resources show the effectiveness of our techniques that were able to reduce the cycle count by 10.2% on average compared to an effective technique in the literature.
- S. Bakz, G. Yaoz, R. Pellizzoni, and M. Caccamo, "Memory-aware scheduling
- M. Kandemir and N. Dutt, "Memory systems and compiler support for mpsoc architectures," Multiprocessor Systems-on-Chips, 2005.
- L. Xue, O. Ozturk, F. Li, M. Kandemir, and I. Kolcu, "Dynamic partitioning of processing and memory resources in embedded mpsoc architectures," in Design,
automation and test in Europe (DATE), 2006.


**Index Terms**

Computer Science  Circuits And Systems

**Keywords**

MPSoC  Allocation  Scheduling  Scratchpad