Abstract

In Deep Sub-Micron (DSM) technology, leakage power dissipation consumes the substantial percentage of the total power dissipation and rises exponentially according to the International Technology Roadmap for Semiconductor (ITRS). Leakage power decreases battery life for the entire portable battery operated device such as mobile phones, laptop and cam coder etc. VLSI design constraints are always area, power and delay. To reduce the leakage power losses several techniques has been proposed that proficiently reduces leakage power dissipation. Leakage power in CMOS VLSI circuits can be controlled at the circuit level. This paper has considered two run time leakage reduction mechanics i.e. Input Vector Control (IVC) and Gate Replacement (GR). When the first technique is applied on the CMOS circuit, 30% average leakage power reduction is achieved where as 46% of average leakage power is reduces due to GR technique. The Maximum leakage reduction is achieved of 41.2% and 73% due to IVC and GR techniques respectively. These techniques have been applied on ISCAS benchmark circuit C17 using TSMC0.18um technology file on HSPICE simulator.
A Combined Approach of IVC and GR for Leakage Power Reduction in CMOS VLSI Digital Circuit

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Index Terms

Computer Science  Circuits And Systems

Keywords
Leakage current  Deep Sub Micron technology  IVC  Gate Replacement