A 2.4 GHz Low Noise Amplifier in 0.18μm CMOS Technology

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ABSTRACT
In this paper, design of a 2.4 GHz low noise amplifier (LNA) intended for use in wireless telemetry telecommand system for satellites is presented. The design has been done in 0.18μm UMC RF CMOS process. The amplifier provides a forward gain (S21) of 16.63 dB with a noise figure of only 1.25dB while drawing 5.4mW from 1.8V supply in single ended configuration. Its differential counterpart also presented which has S21 of 20.34 dB with 1.45 dB noise figure and 4mW power consumption.

General Terms
RF CMOS, VLSI Design, Wireless.

Keywords
LNA, low-noise amplifier (LNA), noise figure, Gain.

1. INTRODUCTION
CMOS has become a competitive technology for radio transceiver implementation of various wireless communication systems due to technology scaling, higher level of integrability, lower cost, etc. [1], [2].The main advantage of using CMOS for RF frontends is ease of integration with digital section leads to whole system on a single chip.

The LNA designed is for use in wireless telemetry telecommand system for satellites. It has a number of sub-systems consisting of various sensors and actuators. One such sub-system is the master transponder which is earth facing and communicates with the earth station. All other sub-systems are accessed through this master unit. The information gathered from various sub-systems is relayed to the earth station via the telemetry unit (TM-MASTER). The earth station sends commands to control and configure the various sub-systems, via the telecommand (TCMASTER), both these happen through the respective Master units. Here the commutation should be through wireless as it has advantages like less weight of satellites etc. and it is based on IEEE 802.15.4 which is popular for wireless sensor networks.

Typically the first block of a receiver is LNA [3]. The overall performance of receiver depends on the LNA noise figure and gain.LNA design is such that it should provide minimum noise figure (NF) while providing gain with sufficient linearity (typically measured in terms of the third-order intercept point), IIP3 and providing a stable 50Ω input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier. A good input match is even more critical when a preselect filter precedes the LNA because such filters are often sensitive to the quality of their terminating impedances. In addition the standard used for implementation of communication system is low data rate, low power and usually each node is operated with battery. So, the design of LNA is aimed at lower power consumption.

This paper organized as, section 2 give typical LNA architectures, section 3 presents classical LNA design, section 4 gives complete details of inductive source degenerated LNA, section 5 gives noise figure optimization techniques and section 6 explains about the designed LNA and simulation results also presented.

2. LNA ARCHITECTURES
Based on the way input matching is provided LNA can be classified into four architectures [3]. Resistive termination, 1/gm termination, shunt-series feedback and inductive degeneration respectively as shown in the Figure 1.

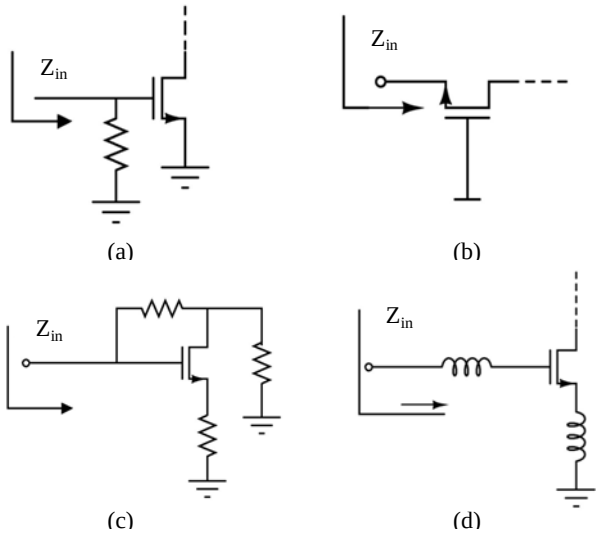

Figure 1. Common LNA Architectures (a) Resistive Termination (b) $1/g_m$Termination (c) Shunt-Series Feedback (d) Inductive Degeneration

Among all these inductive degeneration has the lowest noise figure and it is very popular for narrow band design. As the system comes under narrow band applications we have selected inductive source degenerated LNA. It also has the advantage of high gain, explained in the upcoming sections. $1/g_m$ or the common gate topology offers less gain and poor noise figure

compared inductive degenerated. Other architectures are very poor. Common gate topology is popular for wideband designs; gain can enhance through using gain boosting circuitry.

3. CLASSICAL DESIGN

In the classical design LNA is treated as a two port network [4]. A noisy two-port network being driven by a noisy source can be equivalently represented as two port network with input referred noise voltage and current sources. The noise factor (noise figure is noise factor expressed in dB) is defined as

$$F = \frac{SNR_{OUT}}{SNR_{IN}} = \frac{total\ output\ noise}{total\ output\ noise\ due\ to\ source}$$

The equation (1) gives the noise factor of such network

$$F = 1 + \frac{G_U + |Y_C + Y_S|^2 R_n}{G_S} \quad (1)$$

where Y_s and Y_c are the source admittance and correlation admittance respectively. The minimum noise factor can be solved for by first taking the derivative of equation above with respect to the source conductance and susceptance and setting them equal to zero. This gives the optimum source admittance for which minimum noise figure is possible. So, the noise factor equation becomes

$$F = F_{min} + \frac{R_{in}}{G_S}\left[\left(G_S - G_{S,opt}\right)^2 + \left(B - B_{S,opt}\right)^2\right] \quad (2)$$

This optimum source admittance is usually different from that of source impedance for which maximum power transfer is possible. And also it doesn't give any information regarding power consumption. In the next sections inductive degenerated LNA is analyzed addressing all the mentioned issues.

4. INDUCTIVE SOURCE DEGENERATED LNA

4.1 Impedance Matching

Figure 2 shows the cascade inductive degenerated LNA. L_s is the source inductor and L_g is the gate inductor. The expression for input impedance can be given by equation (3)

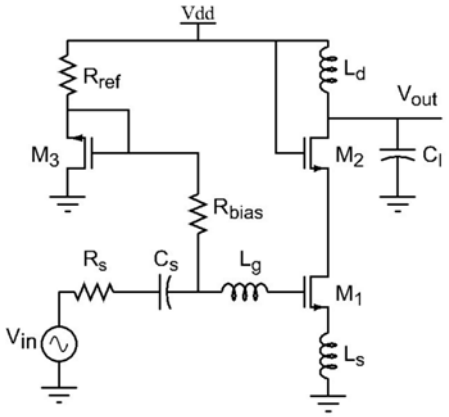

Figure 2. Cascode Inductive Degenerated LNA

$$\cdots \quad j\omega C_{gs} \quad C_{gs}$$

where C_{gs} is the gate-source capacitance, g_m is the device trans-conductance and ωT is the unity current gain frequency (transit frequency). At the series resonance of the input circuit, the impedance is purely real and proportional to L_S. By choosing L_S appropriately, this real term can be made equal to 50Ω.As in the chip LNA drives directly the mixer so there is no need of 50Ω output impedance matching. As it can be seen that a stable 50Ω input impedance dependence on g_m, it can be achieved through constant gm biasing. In this and the all the subsections equations are derived without considering M_2. It doesn't affects noise performance but increases gain and linearity.

4.2 Gain

The quality factor of the input circuit at resonance is given as

$$Q_{in} = \frac{1}{\omega_0\left(R_s + \frac{g_m L_s}{C_{gs}}\right)C_{gs}} \quad (4)$$

$$Q_{in} \approx \left(\frac{\omega_T}{\omega_0}\right)\frac{1}{2R_s}$$

where ω_o is the resonant frequency. At resonance, the voltage across the capacitor is equal to

$$v_{gs} = Q_{in} v_s \quad (5)$$

Hence the effective transconductance can be given as

$$G_m = \frac{g_m}{\omega_0(R_s + \frac{g_m L_S}{C_{gs}})C_{gs}} \quad (6)$$

Here the transconductance is boosted, hence inductive source degenerated offers high gain. This boosting affects the linearity of the LNA. Finally the voltage gain expression can be given by equation (7).

$$A_v = \left(\frac{\omega_T}{\omega_0}\right)\frac{R_L}{2R_S} \quad (7)$$

4.3 Noise Factor

4.3.1 Due to Thermal Noise Alone

Figure 3 shows the small signal model for noise factor calculation. The noise factor, considering the channel thermal noise as the main source of noise source the noise factor [3] can be given by equation (8)

$$F = \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_S \left(\frac{\omega_O}{\omega_T}\right)^2 \quad (8)$$

Where R_l is the gate inductor resistance, R_S is the source resistance, γ is the channel thermal noise, g_{d0} is the transconductance when V_{ds} is equal to zero. R_g is the distributive gate resistance.

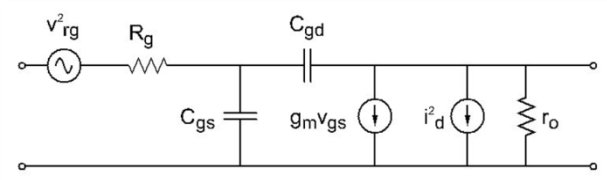

Figure 3. Small Signal Noise Model

Neglecting the inductor resistance the noise factor equation becomes

$$F = 1 + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (9)$$

Observing the equation noise factor depends on the quality factor of the input circuit. Thus increasing the quality factor of the input circuit improves the noise factor at the same time it affects the linearity.

4.3.2 Due to Thermal Noise Alone

If the device is biased so that the channel is inverted, fluctuations in the channel charge will induce a physical current in the gate due to capacitive coupling [3]. Taking this induced gate noise in to account the small signal model for noise calculations is shown in Figure 4.

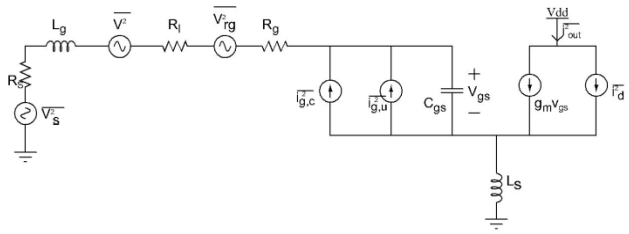

Figure 4. Complete Noise Model

The noise factor can be give as [5]

$$F = 1 + \frac{Rg}{R_s} + \frac{\gamma}{\alpha}\partial g_m R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (10)$$

where $\alpha \equiv g_m/g_{d0}$ and χ is given by

$$\partial = 1 + \frac{2|C|}{\omega_0 R_s C_{gs}}\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + \frac{1}{(\omega_0 R_s C_{gs})^2}\right) \quad (11)$$

Where c is the correlation coefficient, has value j0.395. Observing F is not simply depends on Q, but it both directly proportional and inversely proportional to Q. Hence there exists a particular value of Q for which minimum noise figure is possible. Usually referred to as optimum quality factor of the input circuit Q_{opt}.

4.4 Linearity

An important metric of linearity in narrowband amplifier design is the input third order intermodulation point (IIP3) of the circuit.IIP3 of the circuit in Figure 2 Can be given as [5]

$$IIP_3(dB_m) = IIP_{3,in}(dBm) - 20\log_{10}\left(\frac{1}{\omega_0 C_{gs} R_s}\right) \quad (12)$$

where an input match is assumed. The first term in equation (12) is the intrinsic IIP3 of the device, and arises from the fact that short channel CMOS transistors exhibit velocity saturation, which gradually linearizes the ideal quadratic of the long channel drain current equation. The second term results from the extra voltage boost across the C_{gs} due to the series tank. This inductive degenerated CMOS LNA has the advantage of the high gain because of the Q boosting effect and also at the same time it affects the linearity of the overall amplifier. Since, the signal across gate-source is quality factor times the input signal.

5. NOISE FIGURE OPTIMIZATION TECHNIQUES

5.1 Impedance Matching

As explained in section 3, amplifier is treated as two-port network, and it attains minimum noise figure if the source admittance is equal to the optimum source admittance. Hence the optimization involves in the design of impedance matching network as shown in the Figure 5.

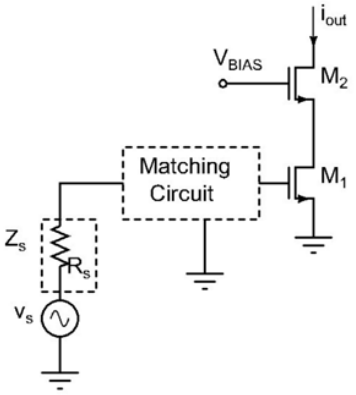

Figure 5. Matching Circuit

This transforms the source impedance to the optimum source impedance that gives the minimum noise figure. The expression for the optimum source admittance can be given [7] by the equation (13)

$$Y_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1 - |c|^2)} - sC_{gs}\left(1 + \alpha|C|\sqrt{\frac{\delta}{5\gamma}}\right) \quad (13)$$

It can be seen that the optimum source admittance for input matching is inherently different from that of the noise matching in both real and imaginary parts. Thus one cannot obtain both input matching and minimum noise figure simultaneously.

5.2 Other Optimization Techniques

Using the inductive degenerated topology power match and input match can be achieved through properly selecting source inductor and gate inductor values. Considering the induced gate noise the optimum noise figure can be achieved for a optimum input quality factor [5] given by equation (14)

$$\omega_{opt} \approx \frac{1}{3\omega C_{OX} R_s Q_{in,opt}} \tag{14}$$

where

$$Q_{in,opt} = |c| \sqrt{\frac{5\gamma}{\delta}} \left(1 + \sqrt{1 + \frac{3}{|C|^2}\left(1 + \frac{\delta}{5\gamma}\right)} \right) \tag{15}$$

In equation (15), represents the gate–oxide capacitance of the MOSFET per unit area. The minimum NF in this case can be given by

$$F_{min} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right) \tag{16}$$

Using the equation (14) results in very high value of width sometimes it is not practically realizable even then it results in high power consumption.

To reduce the power consumption an external capacitor C_{ex} (as shown in Figure 6) which has value equal to C_{gs} can be added to reduce the power consumption without effecting linearity and noise performance.

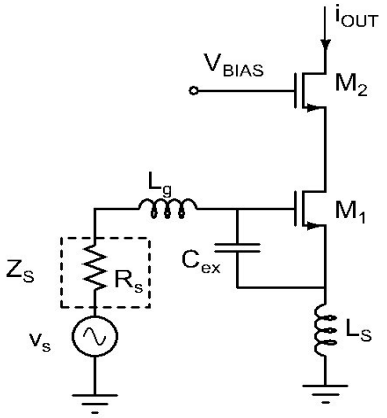

Figure 6. Cascode LNA with External Capacitor

6. LNA DESIGN

Figure 7 shows the schematic of designed single ended LNA. M_1 is the main transistor and the M_2 is the cascode transistor. This circuit uses two more additional transistors than in the basic LNA. They are used to improve the linearity through feed forward technique [8]. Using equations (3) L_s, L_g values are estimated. Exact tuning can be achieved through repeated simulations. L_d value depends on the load capacitance at which it resonates.

The sizing of the input device is of utmost importance since it has the greatest impact on the LNA figures of merit. Gm and NF *vs* width of the device plots while keeping the resonant frequency and bias current constant are helpful in finding out the optimum device width. This can also be achieved through repeated simulations.

The purpose of the second stage of the low noise amplifier is to further increase the gain. Increasing the length of the transistor also helps to improve the isolation as well. Furthermore, it helps in reducing the effect of C_{gd} of the main transistor [9].

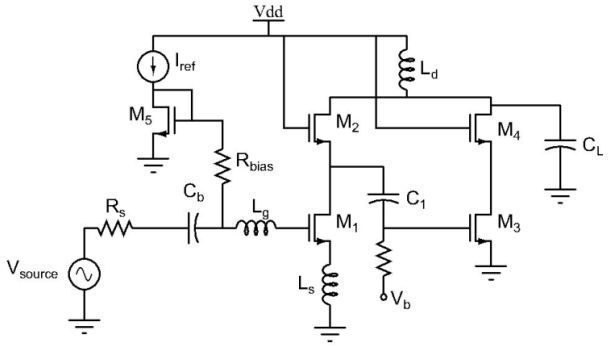

Figure 7. Single Ended LNA

For the differential ended design also follows the same procedure as single ended. The differential schematic is given in the Figure 8.

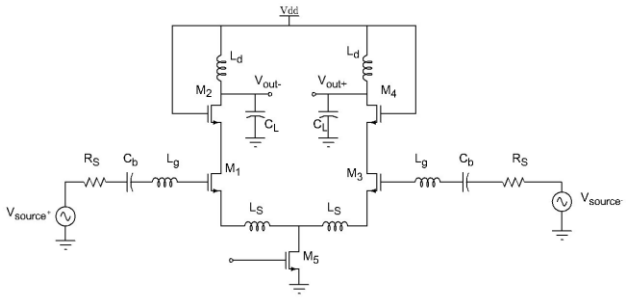

Figure 8. Differential Ended LNA

For the differential implementation of LNA a balun is needed at its input to convert the coming single ended signal into differential ended signal.

In neither of the designs output matching is not considered as LNA directly drives the mixer in the chip. If the mixer is a differential ended and LNA is single ended again balun is needed in between these to convert single ended signal into differential ended. This can be implemented with on chip active balun.

6.1 Simulation Results

The design was simulated using the BSIM3 models provided for the UMC 0.18 µm RF CMOS process. The following Figures (9-12) shows the S21, Noise Figure, IIP3, stability factor of

single ended alone. Table.1 summarizes the performance of both single ended and differential LNAs.

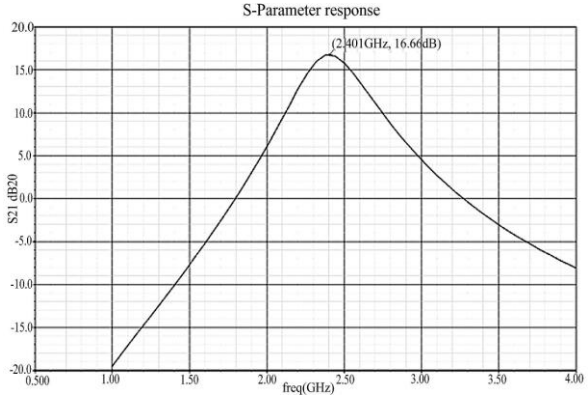

Figure 9. S21

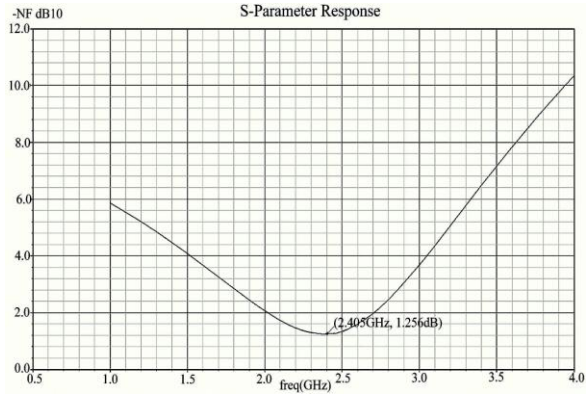

Figure 10. NF

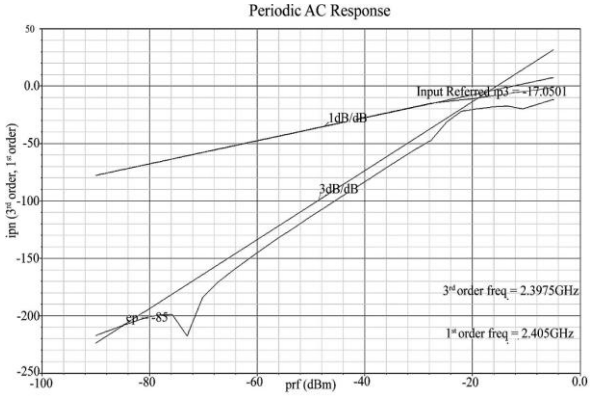

Figure 11. IIP3

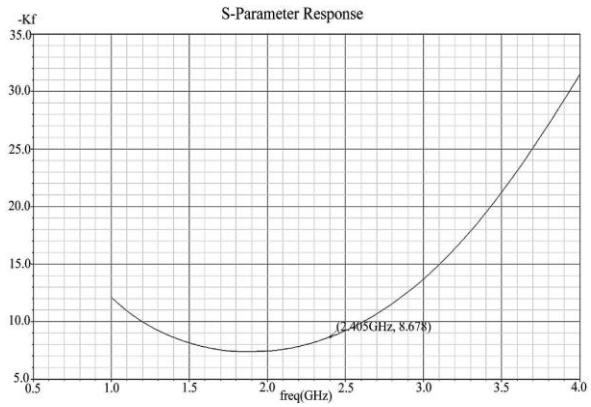

Figure 12. Stability Factor

Table 1. Performance Summary

Parameter	Single Ended	Double Ended
Frequency	2.4 GHz	2.4 GHz
Power Supply Voltage	1.8 V	1.8 V
Power Consumption	5.6 mW	4 mW
S21	16.66 dB	20.57 dB
Noise Figure	1.25 dB	1.42 dB
IIP3	-17.05 dBm	-28.13 dBm

7. ACKNOWLEDGMENTS

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