CMOS Implementation of
Serial Flash Analog to Digital Converter

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ABSTRACT

Serial Flash Analog to Digital Converter (ADC) is a topology which uses only N number of comparators for N bit ADC. The said converter is developed and implemented in CMOS for 6 bit resolution. The simulation results are presented for TSMC 0.35 um CMOS technology

General Terms

Flash, CMOS, Analog to Digital Converter, conversion time.

Keywords: VLSI, Fuzzy Logic, FPGA

VLSI, PMOS, NMOS, ADC, DAC

1. INTRODUCTION

The conventional flash or parallel analog to digital converter is the fastest converter topology available today. However the hardware requirement for it increases exponentially as the number of bits increase. The number of comparators required for N bit ADC is $2N - 1$ [1] [2].
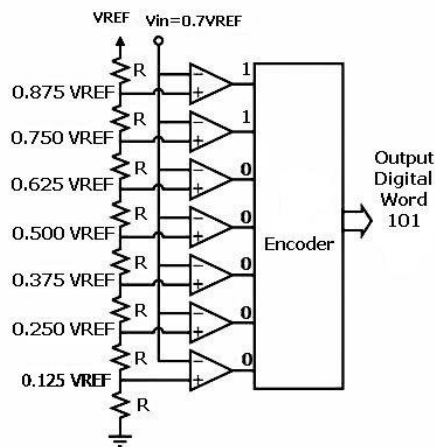

Fig.1 Schematic for Flash AD Converter

The number of resistors is also same as number of comparators. In CMOS technology, these resistors also occupy significant area. Hence Flash ADCs are implemented up to 8 bits resolution. The output of flash converter is typically thermometric code which is converted to binary code using an encoder. The typical schematic for Flash converter is shown in Fig 1.

The successive approximation analog to digital converter uses successive approximation register which is essentially synchronous sequential machine. The conversion time for N bit ADC is N T seconds, where T is time period of the clock. As can be seen the hardware requirement is less, only one analog comparator and N bit DAC is required. In addition to digital logic for successive approximation register. Typical schematic for such ADC is shown in Fig 2. It is possible to realize asynchronous version for SAR converter [5].
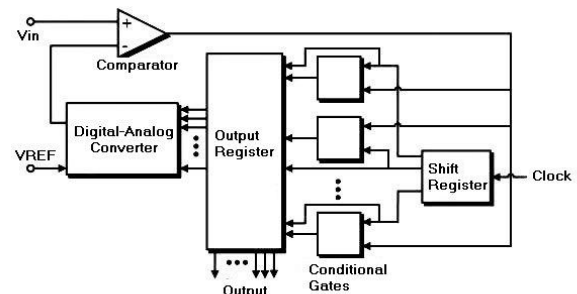

Fig. 2 Schematic for Successive Approximation ADC

The proposed serial flash conversion technique uses N number of comparators for N bit resolution [3] [7].

2. BUILDING BLOCKS FOR PROPOSED ADC

The blocks required for the proposed ADC are weighted current mirrors, current switches and comparators. The current sources in CMOS technology use two MOS transistors and the multiplication factor of the current depends on W/L ratio of the transistors used. Simple MOS current mirror topology is employed in the proposed ADC. However for higher bit resolution ADCs, cascode current mirrors are preferred [4].

The current steering switch is controlled by output of the comparator and an inverter. The current is either allowed to flow into MOS transistor which is used as resistor or is steered to ground depending on the output state of the comparator.

The CMOS comparator uses PMOS differential pair to achieve input common mode range from 0 to 2.1 volts for supply voltage of 3.3V. The comparator used is designed to give input

resolution of 3 mV. The comparator can resolve 2100mV/3mV ie 700 steps which exceeds requirement for proposed 6 bit resolution. The inverter is formed using transistors M10 and M11. It gives sharper transitions and to rail to rail output. The designed circuit is shown in Fig. 3.
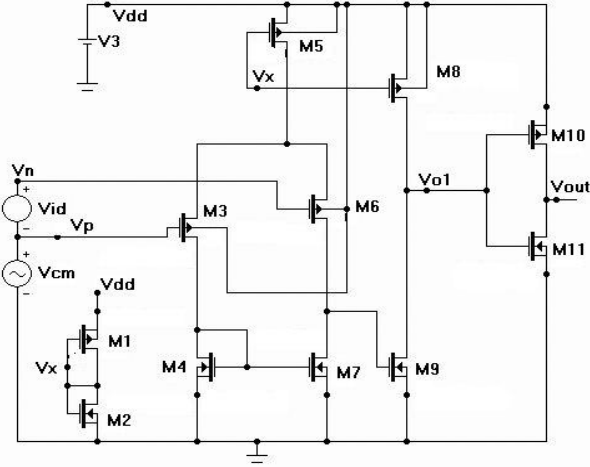
**Fig.3 PMOS Input Comparator with 3mV Resolution**

The circuit shown in Fig. 4 has PMOS M1 as current source. NMOS transistors M3 and M4 act as a switch. The current from M1 flows into NMOS M6 if M3 is ON or flows to ground if M4 is ON. M2 and M5 form an inverter. The switch is controlled by output of the comparator Vb_0. If output (Vb_0) is high, then the current flows into MOS transistor M6. If output of comparator is zero then it flows to ground. The current of PMOS M1 is decided by its gate voltage Vg, the voltage is set to constant value of 2.4 V. It ensures that the transistor remains in saturation. The transistor M6 is working in linear region as Vg=2.4 V. The output voltage Vro will be limited to full-scale voltage of 210mV.
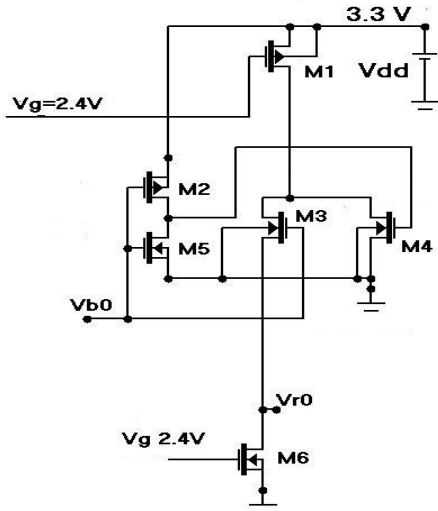
Fig. 4 Circuit for Current Mirror and Steering Switch

The bias source voltage Vg is realized by using two transistors. The voltage VG is decided by W/L ratios of NMOS and PMOS transistors.

3. CONVERSION PRINCIPLE
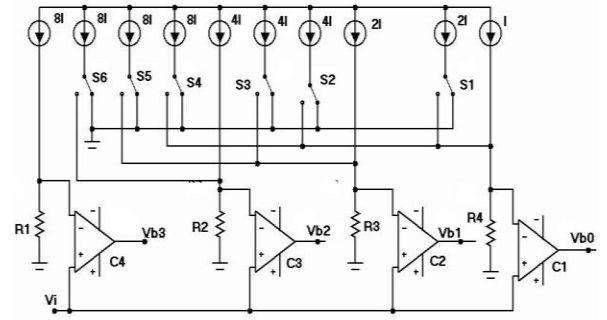
Fig. 5 Schematic for Serial Flash ADC

The Fig. 5 is block-schematic for 4 bit version of the proposed analog to digital convertor. Note that the clock is not required. For analog to digital conversion, number of comparators used is only N= 4 and incase of flash converter we need $2^N-1 = 7$ comparators. The thermometric to binary code conversion is eliminated in the proposed scheme. However the number of weighted current sources is factorial n (n!). and number of switches required is factorial n-1 ((n-1)!). As can be seen the increase in hardware is not exponential with number of bits.

The algorithm for the proposed ADC is based on the fact that successive approximation register ADC can be developed using N number of N bit DACs and N comparators without using successive approximation register. Further it is possible to show that all bits of these DACs are not required to realize this function [3]. The algorithm is developed on this basis.

Consider a case where Vi= 0V. Outputs of all comparators are Low and all the switches ground the current from current sources. The current through R1 through R4 is 8I, 4I, 2I and I, respectively. The four comparators will compare input with four different reference voltages. All the resistors have same value so $Vr0= IR4= V_{LSB}$, $Vr1 = 2 V_{LSB}$, $Vr2=4 V_{LSB}$, $Vr3=8 V_{LSB}$. All these voltages being greater than zero and connected to inverting terminal of comparators, the output of these comparators will continue to remain zero.

The algorithm for N bit ADC can be stated as under

Let $Vr0(t) = V_{LSB}$, $Vr1(t) = 2 \times V_{LSB}$ $Vr2(t) = 4 V_{LSB}$ and $Vr3(t) = 8 V_{LSB}$. Or, in general, set $Vr(n-1)(t) = 2^{(n-1)} V_{LSB}$ for n=0 to N. Set n = N, number of bits. V_{LSB} is step size of ADC.

Step 1 Compare input voltage with Vr(n-1)(t) of comparator C(n).

    X= n
    Y=0
If Vi > Vr(n-1)(t)   Keep output of C(n) comparator High
        While X > 0
            Vr(Y) (t+1)= Vr(Y) (t)+ 2 $^{(n-1)}$ V_{LSB}
                    Y=Y+1
                    X=X-1

    End while

Else output of C(n) will be LOW
While X >= 0
Vr(Y) (t+1)= Vr(Y) (t)
                Y=Y+1

X=X-1

End while

End if

Step 2 t=t+1, n=n-1

Step 3 if n=0 goto step 4

Else go to Step 1

Step 4 Stop

We demonstrate the working of the algorithm with an example(N=4). Let V_{LSB} = 10mV and Vi = 105 mV. Assume that initially Vi=0 and then changes to Vi= 105 mV. When Vi=0, outputs of all comparators will be LOW as explained earlier. Values of Vr0 =10 mV, Vr1 =20mV vr2 = 40mV and Vr3=80mV. When Vi goes to 105mV

Iteration 1 n=4

Step1 (Vi=105mV)> vr3(t)(80mV), c4=high

And Vr0(t+1) = 10mV + 80 mV = 90mV

Vr1(t+1) = 20mV + 80 mV = 100mV

Vr2(t+1) = 40mV + 80 mV = 120mV

Step 2 n=n-1 =4-1=3, t=t+1 goto step1

Iteration 2 n=3

Step1 (Vi=105mV)> (vr2 (t)=120mV),

No c3=LOW

No change in previous values of Vr

So Vr0(t+1) = 90mV

Vr1(t+1) = 100mV

Step 2 n=2, t=t+1 goto step1

Iteration 3 n=2

Step1 (Vi=105mV)> vr1(t)=100mV),

YES c2=High

Change in previous values of Vr with $2^{(n-1)}$ V_{LSB}= 20mV

And Vr0(t+1) = 90mV+ 20mV

=110mV

Step 2 n=1, t=t+1 goto step1

Iteration 4 n=1

Step1 (Vi=105mV)> vr1(t)=110mV),

No c1=Low

No change in previous values of Vr

Step 2 n=0, t=t+1 goto step4

Step 4 stop

As can be seen outputs of comparators C4C3C2C1 will be

1010. This is equivalent of 10 in the range of 0 to 15. The time t and t+1 indicate the next value of the output after the delay of the comparators. If there is no change then that delay will be zero. As can be seen, the output settles after maximum of n transitions. This transition delay is decided by comparator delay. Thus maximum time for coversion will be

Conversion time = (N) (Tcomp), where Tcomp is comparator delay.

The conversion time for this ADC is limited by above mentioned delay. Note that the clock is not required to resolve different bits. Since the resolving of the bits is done sequentially from MSB to LSB, the topology is named as asynchronous serial flash ADC. When this converter is used as tracking converter then the conversion time will be much less, as changes will be in the LSB comparators.

4. RESULTS

6 bit asynchronous serial flash analog to digital converter circuit is implemented and simulated for 0.35um TSMC SCN035 CMOS technology using level 8 (Level 7 for Pspice) spice model for PMOS and NMOS devices. The ramp input voltage Vi is applied from 0 to 220 mV. The waveform for the same is shown with outputs Vb_0 Vb_1 and Vb_2 in Fig. 6 and Vb_3 Vb_4 and Vb_5 in Fig. 7.

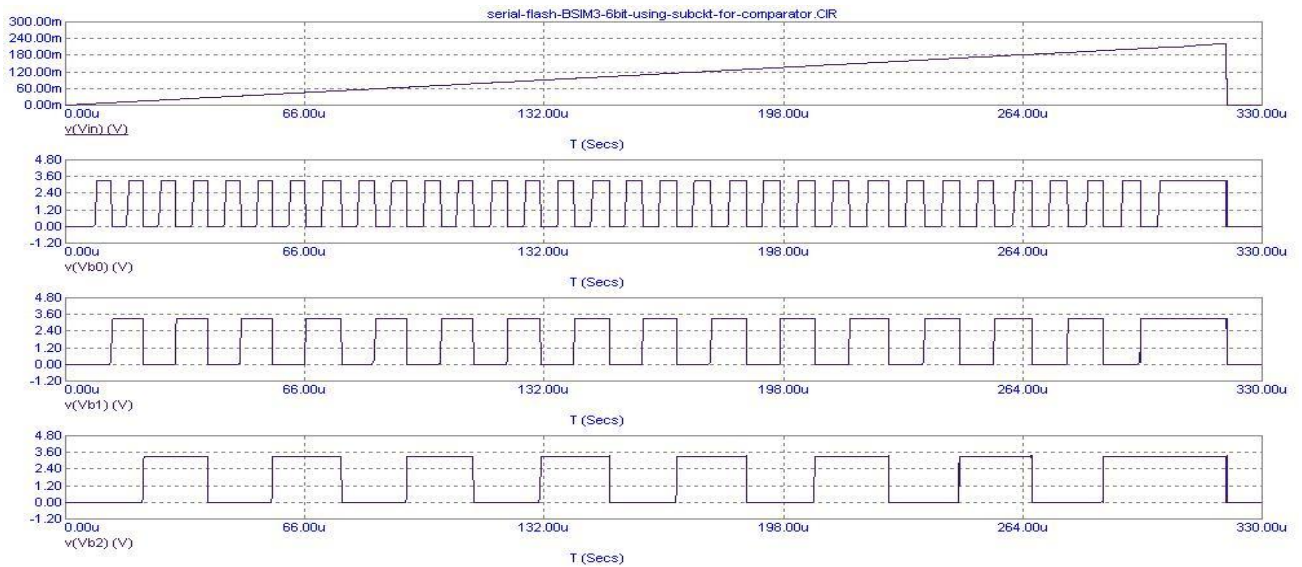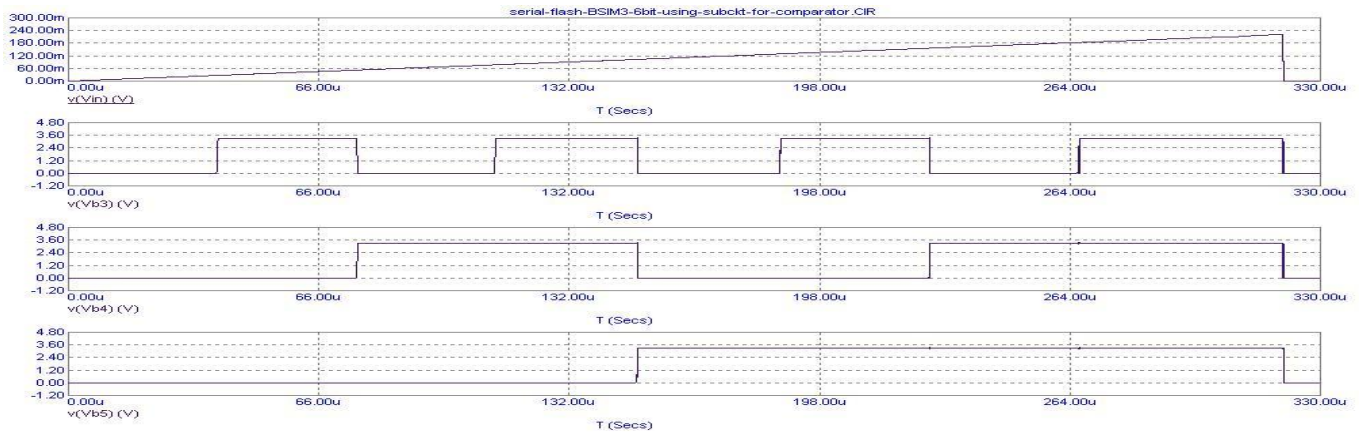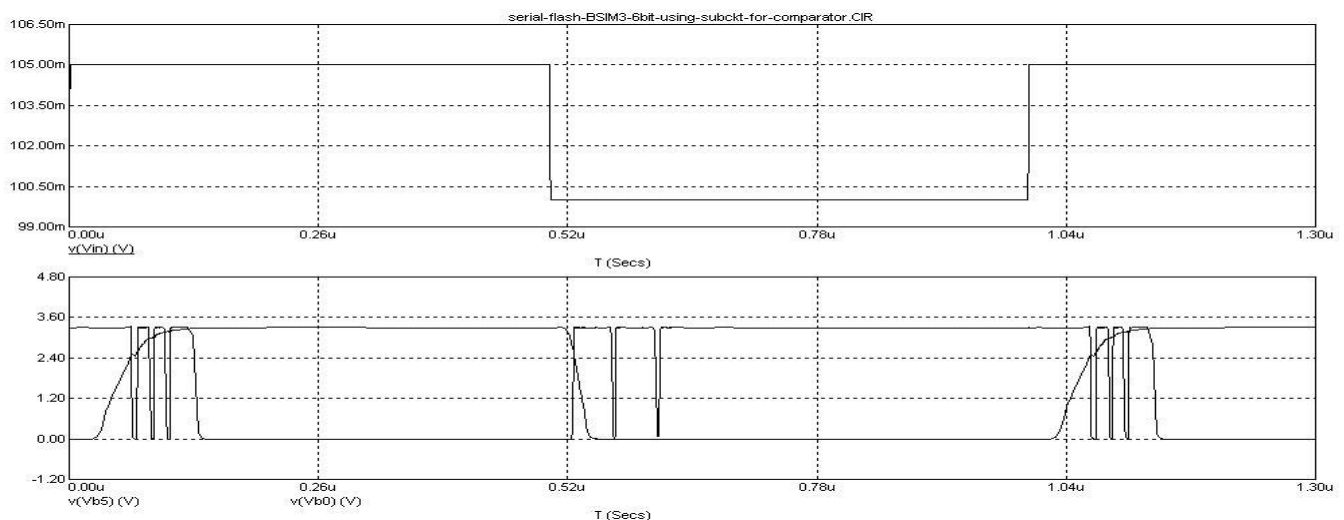**Fig. 6 Output Bits Vb$_0$,Vb$_1$,Vb$_2$ for Vin= 0V to 220mV**

Fig. 7 Output Bits Vb₃, Vb₄, Vb₅ for Vin= 0V to 220mV

Fig. 8 Conversion time for output change from 100000 to 011111 and back to 100000

Note that the maximum conversion time of ADC is observed when output changes from 011111 to 100000 and back to 011111is shown in Fig. 8. The observed maximum delay is 120 ns

Measurement for differential nonlinearity is plotted as in Fig. 9 and is less than ±0.5 LSB ie ± 1.5 mV.
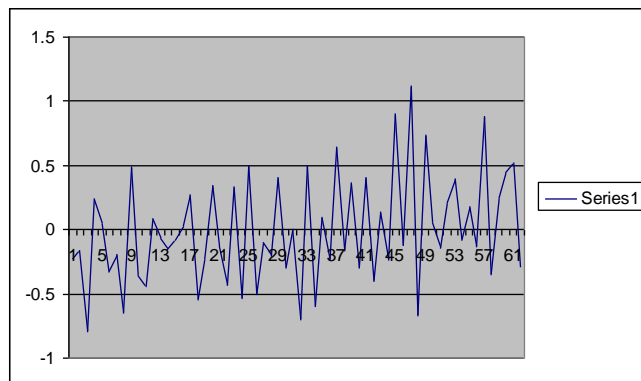
Fig. 9 Differential nonlinearity

The specifications for the converter is summarized in table 1

Sr. No	Parameter	Values
1	Vdd	3.3 V
2	Resolution	6 bits
3	Maximum conversion time	120 ns
4	Power dissipation	4.36mW
5	DNL	$< \pm 0.5$ LSB
5	V_{LSB}	3 mV

Table 1

5. CONCLUSION

An Asynchronous serial Flash converter is implemented and simulated for 0.35 micron CMOS technology. The results are satisfactory. The weighted current sources need to be designed, individually, as W/L ratios are not exact multiples. This is always the case in analog CMOS design. The conversion time can be further reduced by using fast comparators.

6. REFERENCES

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