Design of High Performance PLL using Process,Temperature Compensated VCO

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ABSTRACT
In this paper the Design and Verification of High performance PLL is presented and implemented at 180nm CMOS Process Technology**.** Process and Temperature Compensation Techniques for minimizing the variation of the free-running frequency of Voltage Controlled Oscillator are discussed**.** Matched up and down currents Charge Pump is designed**.** 2 types of PFDs are presented with their consequences. Type 1 PFD is designed with more area and zero dead zone which is compared with type 2 PFD which is designed with less area but 0.01n sec dead zone. The PLL is operated at 1.25GHz with power supply of 1.8V.

General Terms
Phase Frequency Detector, Phase lock loop.

Keywords
Charge pump, loop filter, process voltage and temperature (PVT), ring oscillator, voltage controlled oscillator**.**

1. INTRODUCTION
Phase locked loops (PLLs) are essential building blocks for almost all Integrated Circuits. A Phase-locked loop (PLL) is the most widely used Mixed-Signal Circuit block in a system-on-chip. Advancements in CMOS process technology have enabled circuits to be realized at low power and high performance. But, along with these advantages there exist a number of undesirable traits, such as a high degree of process and temperature variability, high leakage and low dynamic range due to low supply voltage. This paper discusses the impact of these effects in designing Analog Phase-locked loops in Nanometer CMOS.

Continuous scaling poses several design challenges for future high performance architectures. Systematic and random variations in process, supply voltage and temperature (PVT) have become a major challenge to future high performance architecture designs. Two main contributors to on chip variability arise from changes in process parameters and changes in operating temperatures.

VCO is the most important block of the PLL. Since area is dominated by the size of the inductor, LC oscillator does not scale well with technology. Therefore, we propose ring oscillator in our PLL design. Section (2) discusses the issues that are related to Process and Temperature Compensated VCO. The free-running frequency of a ring oscillator is very sensitive to process, voltage and temperature (PVT). Process and Temperature compensation techniques for minimizing the variation of the free-running frequency of an oscillator are considered.

Charge pump and loop filter design is discussed in Section (3). The poor output conductance of short channel devices cause mismatch in the up and down currents. The effects of this on the PLL performance are discussed. Section (4) discusses the phase frequency detector circuit which offers zero dead zone with more number of transistors which is compared with PFD with modified DFFs with more dead zone but less number of transistors. Section (5) gives the simulation results of the PLL and the comparison of PFDs.

2. VOLTAGE CONTROLLED OSCILLATOR
In order to generate a precise frequency, this design is based on the voltage controlled ring oscillator and uses a process and temperature compensation bias technique to improve the oscillator's immunity to environmental variations [4].

2.1 Constant g_m Bias Circuit
Constant Transconductance (g_m) bias circuits are widely used in many analog integrated circuit applications, such as low-noise amplifiers (LNA) and Gm−C filters. If the trans conductance and the reference voltage are process, voltage and temperature (PVT) independent then, naturally, the current generated using these parameters is also PVT independent and hence can be used as a master bias current on a large analog chip.

Resistor-referred constant-gm bias circuit shown in Fig. 2 consists of differential pair with active current mirror [7] consisting of transistors M_{3A} and M_{3B}. While the transistors M_{1A}, M_{2A}, $M_{2B,}$ M_{4B} constitute a cascade current mirror circuit which gives high impedance. The output from this circuit is taken from the drain of the transistor M_{4B}.

Assuming square-law devices and neglecting channel length modulation and body effect, this bias circuit provides a gm that is inversely proportional to resistor R.

2.2 Replica Circuit

The series-connected MOSFETS M_n and M_p generate the reference voltage for a regulator that powers the oscillator as shown in fig 1.

2.3 Two Stage Voltage Regulator

The regulator should suppress external power supply noise to large frequencies and also filter out noise from the reference voltage such as that generated from the constant gm bias circuit.

These conflicting requirements in the Regulator Bandwidth can be met with two stage low-dropout (LDO) voltage regulator [5] for low-power applications is designed without an external capacitor for compensation. With the first stage being a wide band filter that offers good power supply rejection at high frequencies. And the second stage is a very narrow band stage that limits even flicker noise from reference that propagates to the oscillator.

The block diagram of Process and Temperature compensated VCO is shown in fig 1.

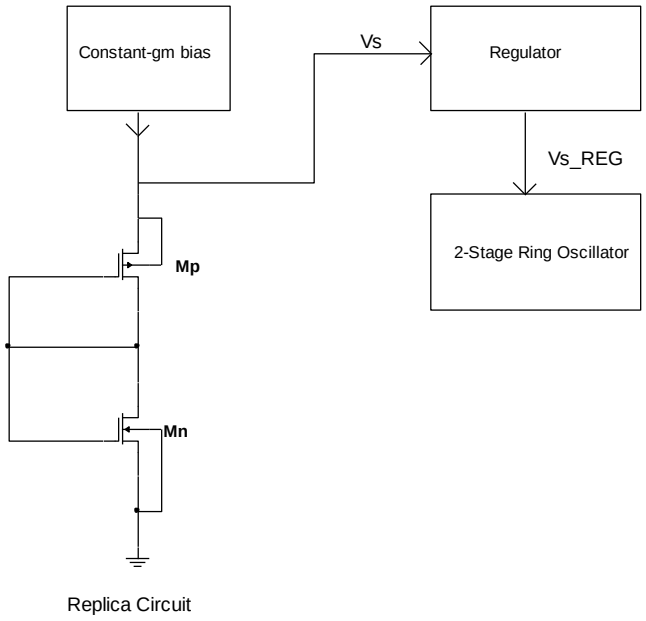

Figure 1. Process and Temperature compensated VCO

The regulator has two stages as shown in fig 3, the first a folded cascode amplifier which allows a lot of gain to be obtained in a single stage consisting of PMOS transistors M_1 and M_2 which act as inputs, with transistors M_9 and M_{10} forming the cascoded tail current source and NMOS transistors M_3 and M_4 are the "folded back" common gate transistors of the cascode. M_5 and M_6 provide the bias currents for M_3 and M_4, respectively. The folded cascode is loaded by an improved Wilson current mirror, formed by M_7, M_8, M_{11}, and M_{12} to improve output resistance of the stage and thus further increases the gain.

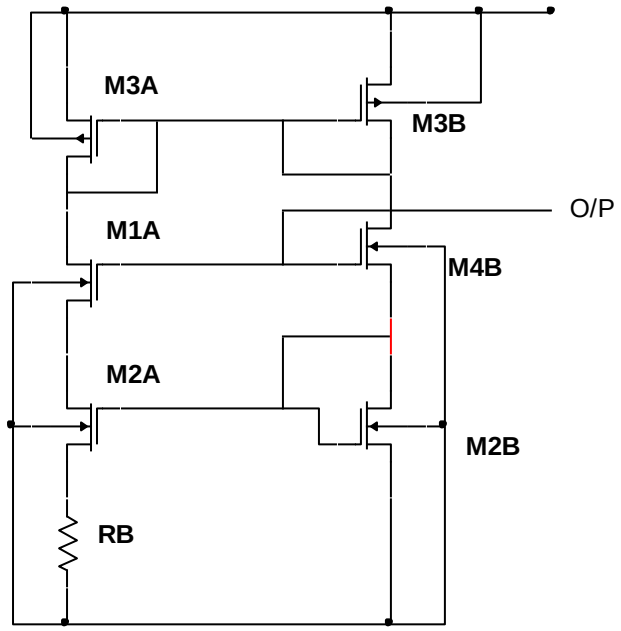

Figure 2. Constant Gm Bias Circuit

The second stage is a large pass transistor acting as a common-source amplifier. This device must be very wide so that it can source large load currents with a reasonable gate-source voltage. The output voltage of the LDO is at the drain of MP, and resistors R_1 and R_2 form a voltage divider to feed a fraction of the output voltage back to the input. Since the first stage is differential, it is less sensitive to power supply disturbances than the second stage, which is single-ended.

The PSRR of the LDO is $20 * \log [A_2 / (1+A_1 A_2 Z)]$

Where A_1 is gain of the first stage, A_2 is the gain of the second stage and Z is feedback factor = $R_2/ (R1+ R_2)$.

2.4 Two Stage Ring Oscillator

An important requirement of ring oscillators, particularly in low-voltage designs, is that the free running frequency be close to the desired value across process and temperature variations to keep the gain of the oscillator low. Such a low gain would minimize the effect of any noise coupling to the oscillator. A two-stage ring is very compact, can produce quadrature clock phases, and has fewer noise sources [6].

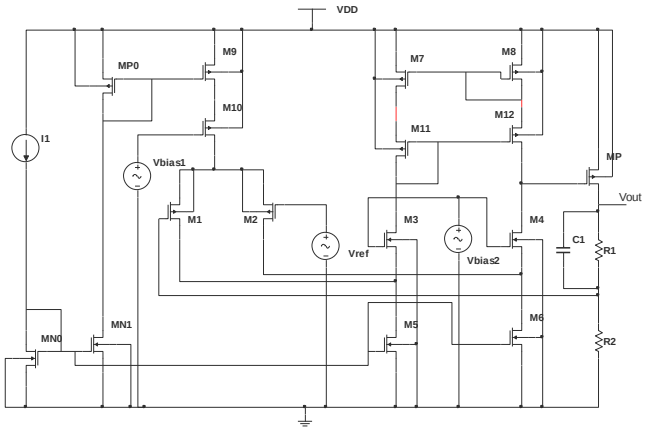

Figure 3. Schematic of Two stage Regulator

The delay element of the ring is a cross-coupled latch with PMOS load as shown in fig 4. The regenerative PMOS transistors provide rail-to-rail output signals via the full switching of the FETs. The latch circuitry reduces the delay of the stage, allowing higher frequency of operation. The full switching of the transistors also reduces the flicker noise.

The transfer function of the latch can be shown to be $\beta / (s - \alpha)$ where $\alpha = (g_{mp}ro - 1) / r_oC_L$, $\beta = g_{mn} / C_L$, g_{mp} and g_{mn} are the trans conductance's of M_p and M_n, and ro is the output resistance at the nodes OP or ON. The input is generally a small disturbance which could be treated as an impulse [1]. The closed loop transfer function of the oscillator is

$$H(s) = \frac{\beta^2}{((s-\alpha)^2 + \beta^2)} = \frac{\beta^2}{s^2 - 2\alpha s + \alpha^2 + \beta^2} \qquad (1)$$

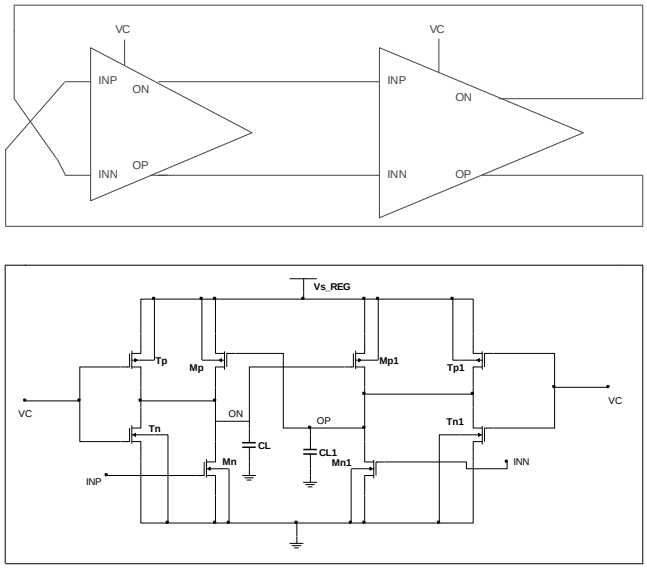

Figure 4. Two stage ring oscillator

The small-signal oscillation frequency is proportional to g_{mn}/C_L where g_{mn} is the Trans conductance of the n-channel driver devices and C_L is the load capacitance. As the gate oxide thickness is one of the most tightly controlled process parameters, the variation of C_L can be less, compared with that of other parameters. Therefore, if the Trans conductance of the n-channel devices in the latch is held constant over process and temperature, we can expect the oscillator to exhibit a nearly constant frequency. An implementation of this scheme, as shown in Figure 1, uses current from a constant-g_m bias circuit applied to two diode connected devices Mn and Mp, which are replicas of the input and feedback devices in the latch.

The dominant parameters that are affected by process variations in a MOS transistor are channel mobility and threshold voltage. As the temperature increases, the mobility decreases, and the current from the constant-g_m bias circuit increases. The threshold voltage has a negative temperature coefficient. The locally generated supply voltage for the oscillator will ensure that the Trans conductance of the n-channel devices at the quiescent point in the latch is held constant over process and temperature.

Simulation results using a 0.13-µm technology are shown in Fig. 5 for a nominal frequency of 1.25 GHz over a temperature range of −40 ◦C to 125 ◦C for five process corners. The maximum frequency spread over process and temperature is about 100 MHz or within 55% of the nominal value. Fig 5 shows the measured free-running frequency from −40 ◦C to 125 ◦C, confirming the validity of the theory and simulations. The error bars show the spread over 15 devices.

3. CHARGE PUMP AND LOOP FILTER

The charge pump is another block that suffers from the low supply-voltage environment. In conventional charge pumps, the poor output conductance of short-channel devices causes mismatch in the up and down currents, as the output voltage deviates from the nominal value of half the supply voltage. In practice, the output voltage range is limited to a few hundred milli volts from either supply rail. Any attempt to drive the output past these limits causes significant mismatch in the up and down currents. This leads to increased reference spurs in the synthesized clock. The circuit shown in Fig. 6 delivers very well matched up and down currents, even when the output is within a few tens of milli volts of the supply rails.

In figure 6**,** the charge pump circuit consists of two current mirrors with a differential amplifier placed between them. The upper current mirror produces the UP current which flows through the upper differential pair transistors and produces UP and UP^1 signals. Similarly the lower current mirror produces the

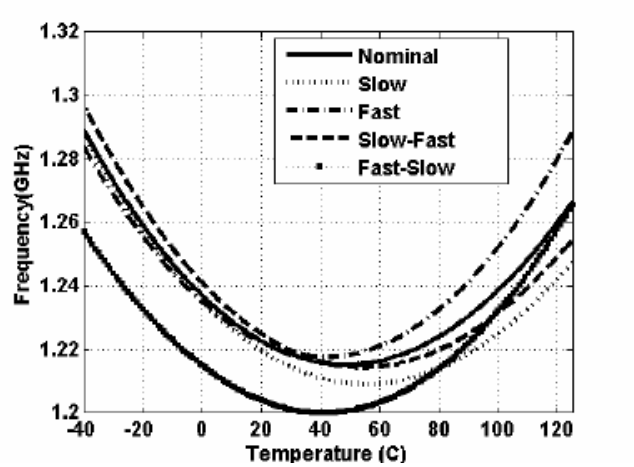

Figure 5. Simulated free running oscillator frequency across temperature and process variations

DOWN signal which flows through lower differential pair transistors and produces DOWN and DOWN[1] signals. The output of the differential pair is given to TUNE in the circuit. While the other end of the output is given to the capacitor C_{dump} which is charged to V_{dump}. Voltage across the C2 capacitor is V_{sense}.

When the PLL is close to lock, the up and down currents flow into dump capacitor Cdump for most of the reference period. Mismatch between these currents results in an effective nonzero average current, which charges or discharges $C_{dump.}$ The rail-to-rail V/I converter compares the voltages across C_{dump} and the loop filter sense node, and adjusts the currents I_{bias} until both voltages are equal and stable. This implies that the average currents into both the loop filter and C_{dump} must reach zero; this is a condition that is met only if the up and down currents are indeed corrected and made equal [1]. Op amp as comparator is used to compare V_{sense} and V_{dump} and give a single voltage to V to I Converter.

A two stage op amp is designed with a single ended output the first stage being a differential amplifier which provides high gain and the second stage provides large swings. The second stage is a simple common source stage so as to allow maximum output swings.

The capacitor C connected between Gate and drain of the transistor M_9 is in the feedback path which provides a feed forward path that conducts the input signal to the output at very high frequencies resulting in a slope in the frequency response. The main purpose of the capacitor is to improve the bandwidth.

A simple passive loop filter consists of a resistor R that is connected in series with a capacitor C1. The resistor influences the bandwidth of the loop, whereas the capacitor controls the damping. To save area, the capacitor may be realized by a MOS device, although it may have large voltage dependence. The capacitor C2 in fig. 6 smoothes large IR ripple on Vcntrl. The output of conventional charge pump is given in fig 7.

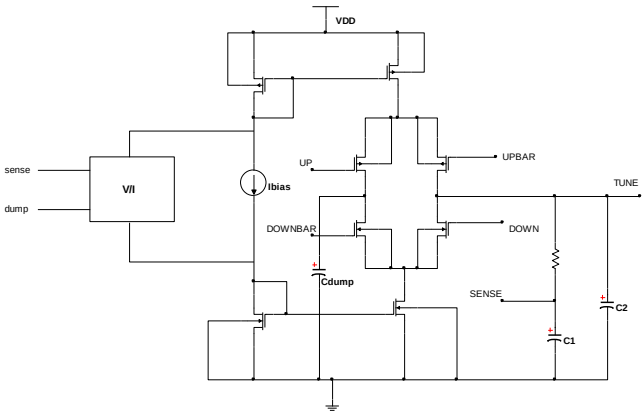

Figure 6. Large dynamic-range charge pump with matched up/down currents filter.

4. PHASE FREQUENCY DETECTOR

The conventional PFD consists of an AND gate and two DFFs. The DFF implementation, being an extensively studied topic, leads to many PFD design alternatives employing modified DFFs or latches for faster operation.

One of the disadvantages that PFD suffers is dead-zone. Dead-zone is a small difference in the phase of the inputs that a PFD will not be able to detect. Dead zone is due to the delay time of

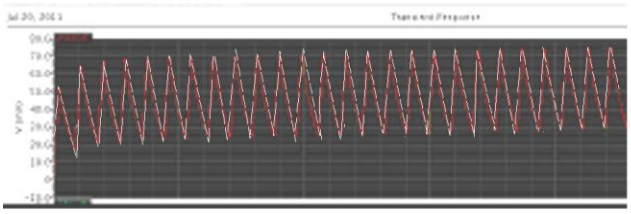

Figure 7. Conventional charge pump output for α = 0.9, R = 6 kΩ, C1= 100 pF, C2 = 2pF and I_{bias} = 100 µA

the logic components and rest of the feedback path of the flip flops. PFD with large dead zone would cause PLL output jittered and the locking time consumed. To minimize the effect of the finite dead zone, gain of PFD must be reduced when PLL is locked and hence a short charging and /or discharging time of the charge pump can be resulted.

We used 2 types of PFDs in our design and achieved almost zero dead zone.

4.1 PFD (type 1)

TSPC DFF is more used in designing DFF of PFD for supporting high speed operation. Double edge triggered DFFs deliver high performance and do not suffer from the problems of charge sharing, charge coupling, reduced voltage swing, poor supply voltage properties and excessive power dissipation plaguing existing DETFFs [8].

Inverters are placed in the PFD to increase the output swing because as V_t is scaled down any circuit driven by a signal which does not achieve a rail to rail swing may experience static power dissipation. Circuits that do not show full swing will fail earlier because the supply voltage needs to be scaled down with the advancement of technology [2].

The transistor sizes in DFF and AND gates were so small in micrometer and because the transistors are used in digital circuitry, the transistors could not switch enough at frequency of 100 MHz. Thus two inverters were placed at the outputs of the UP and DOWN signals in fig. 8 in order to make the signals go to discrete low and high levels (or to improve the output swing).

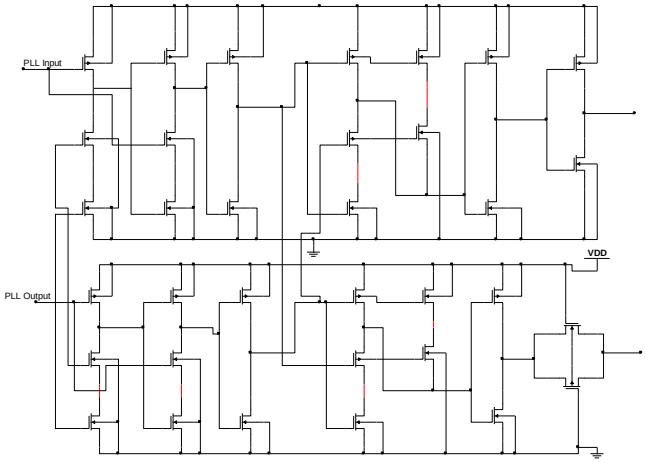

Figure 8. Phase Frequency Detector Circuit (type 1)

4.2 PFD (type 2)

The design consists of two flip-flops and a NOR gate to provide a reset path when both outputs go high at the same time as

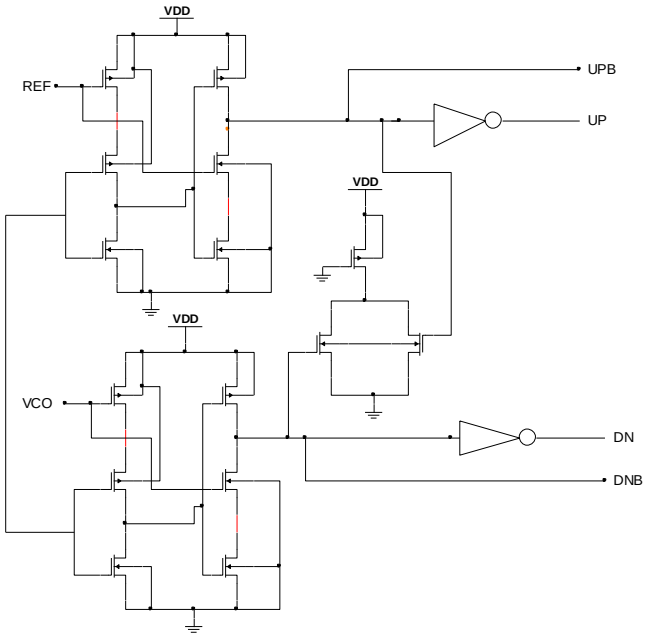

Figure 9. Phase Frequency detector circuit (type 2)

Shown in figure 9. Due to the reset path this design suffers from dead zone. Here true single-phase clock (TSPC) flip-flops are modified and for high-speed operation, a pseudo - NOR gate is used. The reset path is shortened significantly to reduce dead zone significantly [3].

5. SIMULATION RESULTS

For all the blocks and sub blocks of the PLL, schematics are drawn with the help of Cadence tools using TSMC library 180nm CMOS technology. An on-chip clock generation can be made by using a voltage controlled oscillator with a specific control voltage. Some bias techniques have been proposed to compensate for variations in either temperature or process. Hence we use a process and temperature compensation bias technique to improve the oscillator's immunity to environmental variations.

5.1 Conclusion

In this paper temperature process compensated VCO and zero dead zone PFD for high performance PLL has been presented. The design is implemented in 180nm CMOS technology. The circuits are simulated on Virtuoso Cadence tool with GPDK 180nm CMOS technology. The simulation results show that it operates well at high frequency of 1.25GHz with power supply voltage of 1.8V. The PFD designed has nearly zero dead zone.

Table 1 : Simulation Results

F_{REF}	F_{VCO}	PD active pulses	CP output(V)	VCO output(V)
1 GHz	1.25GHz	Down	1.77	1.8
2 GHz	1.25GHz	Up	1.75	1.8
280 MHz	1.25GHz	Down	1.81	1.8
1.25GHz	1.25GHz	None	1.8	1.8
70 MHz	1.25GHz	Down	1.72	1.8

Table 2 Performance Comparison of PFDs

PFD type	Power Dissipation	Current	Number of transistors	frequency	Dead zone
Type 1	1.161mW	0.644mA	34	1.25GHz	Zero
Type 2	4.881mW	2.711mA	19	1.25GHz	0.01ns

6. ACKNOWLEDGMENTS

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