New Efficient 2T and Gate Design

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ABSTRACT

This paper proposes a new design of 2T AND gate. Performance comparison of proposed gate with existing 2T GDI technique is presented. Different methods have been compared with respect to the number of devices, power consumption, power-delay product, temperature sustainability and noise immunity in order to prove the superiority of proposed design over existing 2T gate design. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm technology.

1. INTRODUCTION

Last two decades has seen development of many logic design techniques to improve the performance of logic circuits based on traditional CMOS technology. One form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). Formal methods for deriving pass-transistor logic have been presented for NMOS. They are based on the model, where a set of control signals is applied to the gates of NMOS transistors. Another set of data signals are applied to the sources of the n-transistors [1]. Many PTL circuit implementations have been proposed in the literature [1]-[2], [3]-[7]. Some of the main advantages of PTL over standard CMOS design are 1) high speed, due to the small node capacitances; 2) low power dissipation, as a result of the reduced number of transistors; and 3) lower interconnection effects due to a small area.

However, most of the PTL implementations have two basic problems. First, the threshold drop across the single-channel pass transistors results in the reduced current drive and hence slower operation at reduced supply voltages. This aspect is particularly important for low-power design since it is desirable to operate at the lowest possible voltage level. The second, since the "high" input voltage level at the regenerative inverters is not, the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant [3]. There are many sorts of PTL techniques such as Transmission gate CMOS (TG), Complementary pass-transistor logic (CPL) and Double pass-transistor logic (DPL) that intend to solve the problems mentioned above [4].

Another low-power design technique that allows solving most of the problems of PTL is the gate diffusion input (GDI) technique. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics.

This paper proposes a new design of AND function using two transistors which shows the better performance in terms of power consumption, power-delay product and it is also area efficient as compared to traditional CMOS and CPL AND functions. Existing AND gate designs are briefly described in Section II. Proposed AND cell is discussed in Section III. Results of quantitative comparisons based on simulations of AND gate using GDI logic technique with proposed cell is shown in Section IV and conclusions are finally drawn in Section V.

2. PRIOR WORK

The design of two input AND gate based on traditional CMOS technology consists of six transistors (6T) [1], [2] and [7]. The advantage of this gate is that it gives full output swing i.e.; no threshold loss but on the other side it has many shortcomings such as more area because of six transistors required to design a gate, large power consumption and less speed. For every input combination it produces the delay of 3T.

Similarly the design of AND gate based on CPL technique consists of four transistors (4T) [1]-[2], [3]-[7]. This circuit shows better performance than CMOS AND gate in terms of area, power consumption and speed but it shows threshold loss due to pass transistor logic used.

Fig.1 shows another efficient design of two input AND function reported in the literature. It is based on GDI technique [8]-[11]. Area wise it is the most efficient and fastest AND cell reported in the literature as it uses only two transistors. It also consumes least power but on the darker side it has nearly 10% more threshold loss than CPL AND gate. Therefore the GDI based AND gate is superior to other two designs discussed above.
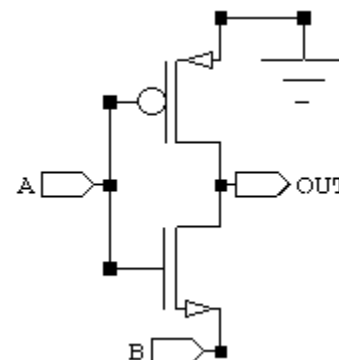

Figure.1 GDI AND gate

3. PROPOSED 2T AND GATE DESIGN

The proposed design of two input AND function is shown in Fig.2. It is a modified GDI AND gate. When AB=00 and 01 respectively, PMOS transistor is ON and NMOS is OFF and as

PMOS is weak '0' device, it will pass incomplete logic low signal to the output. With both the inputs stated above 'A' is constantly zero but 'B' is changing its state from '0' to '1' i.e.; gate voltage at NMOS is less than V_t but as the source voltage is increasing from low to high, it will introduce the DIBL (Drain Induced Barrier Lowering) effect due to which sub threshold current will flow across NMOS and as a result the final output will get affected as shown in Table I. When AB=10, PMOS transistor is OFF and NMOS is ON, and as NMOS is strong '0' device, it will pass complete logic low signal to the output and when AB=11, PMOS transistor is OFF and NMOS is ON, and due to NMOS is weak '1' device, output will be charged to incomplete logic high. The data related to above description is shown in Table 1.

This design proves its superiority over the existing GDI based design in terms of power consumption, power-delay product and threshold loss. It has the delay of only one transistor as for each input combination only one transistor is on between the two and the output is produced.
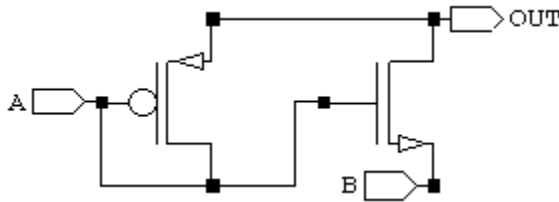

Figure.2 Proposed design of AND gate

The proposed circuit has better noise immunity and temperature sustainability compared to existing 2T GDI AND gate.

Table 1. Truth table of proposed AND gate at 1V amplitude

A	B	Expected Output(Volts)	Obtained Output(Volts)
0	0	0	-0.103
0	1	0	0.1
1	0	0	0
1	1	1	0.898

4. SIMULATION ANALYSIS AND PERFORMANCE COMPARISON

In order to test the performance of proposed AND cell, detailed comparisons are performed. The existing and proposed designs are simulated using BSIM 3v3 90nm technology on Tanner EDA tool. To establish an impartial testing environment, both the circuits are simulated on the same input patterns. Simulation results shown in Fig.3-Fig.6 depicts that the proposed AND cell is the viable option for efficient design.
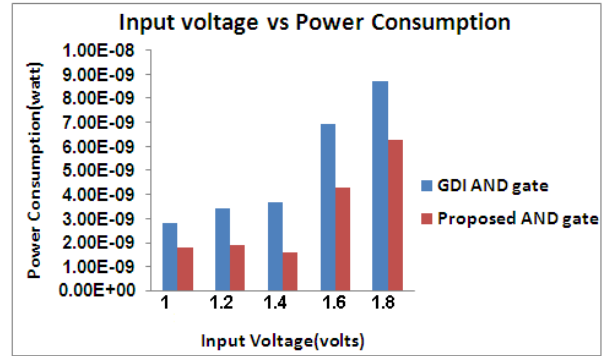

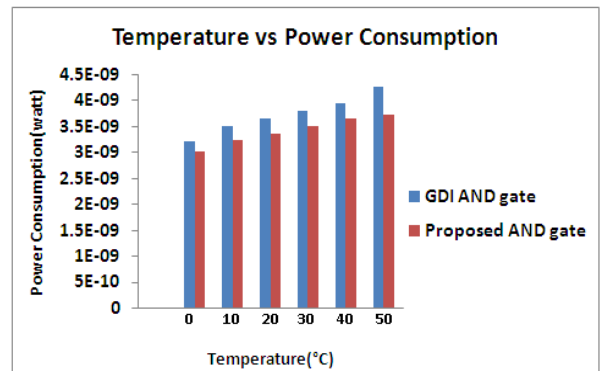**Figure.3 Power comparisons at varying input voltages**

Figure.4 Power comparisons at increasing temperature

Fig.3 and Fig.4 reveals that the proposed design of AND gate has better performance in the terms of power consumption with increasing input voltage and temperature than existing 2T design. Therefore, the proposed design is more temperature sustainable.
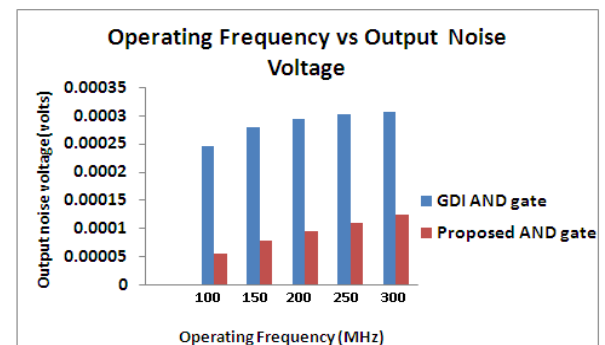

Figure.5 Output noise voltage at varying operating frequencies

Similarly, Fig.5 reveals that the noise immunity of proposed design is far better than GDI based AND gate. Hence, in a nutshell our proposed design is superior to the other AND gate designs reported in the literature.

5. CONCLUSION

This paper proposes a new design of AND function, which resulted in better performance in terms of power consumption, noise immunity and, temperature sustainability. Hence, the

proposed gate can be used for efficient multiplier and other complex designs. All the simulations are carried out at Tanner EDA tool at BSIM3v3 90nm technology.

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