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Design of Multi Threshold (Multi Vth) Level Converters for Block Interfaces

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ABSTRACT
High-performance and low-power are the two main criteria in modern digital design. Level converters are important to transfer low voltage input swing signal among the circuits operating at different voltages to get high voltage output swing signal. Previously feedback level converters suffer from short circuit power and long propagation delay. Multi Vth level converters and multiple supply voltages assignment are used to reduce the power dissipation, propagation delay. The blocks operate at high speed utilizes high supply voltages and blocks operate at low speed utilizes lower supply voltage. To interface these blocks, level converters can be used. Based on this survey a new low power and high performance level converters are proposed.

Keywords
High-performance, multiple supply voltages, multiple threshold voltages, parameter variations, power efficiency, voltage level converters.

1. INTRODUCTION
Technology scaling is the main thrust behind the advancement of CMOS technology. More and faster transistors are crammed onto integrated circuits with each new technology generation. Furthermore, deviation from the constant field scaling due to the non-scaling parameters of the MOS transistors (the thermal voltage, the silicon energy band gap, and the source/drain doping levels) leads to an increase in the power density. The increased power dissipation degrades the reliability, increases the cost of the packaging and cooling system, and lowers the battery life time in portable electronic devices.

An effective method for reducing the power consumption is scaling the supply voltage. Dynamic, short-circuit, and leakage components of power consumption are simultaneously reduced with the scaling of the supply voltage in a CMOS circuit. Lowering the supply voltage, however, also degrades the circuit speed. The supply voltages of the gates on the noncritical delay paths are selectively lowered while a higher supply voltage is maintained on the critical delay paths in order to satisfy a target clock frequency in a multi-VDD circuit.

The previously published level converters rely on some form of feedback circuitry for controlling the operation of the pull-up network transistors in order to avoid static dc current within the level converter. These circuits, however, suffer from significant amount of short-circuit current and degraded speed characteristics due to the typically slow response of the feedback circuitry. Furthermore, to achieve functionality with a very low voltage transmitter, transistor resizing (significant increase in the device widths) is required in these feedback-based level converters, thereby further increasing the power consumption and the propagation delay.

In this paper, three novel level converters based on a multi threshold voltage CMOS technology are presented. Unlike the conventional level conversion techniques based on feedback, the proposed level converters eliminate the static dc current using multi-Vth devices. The new level converters are compared with two previously published feedback-based level converters for different supply voltages. The effectiveness of the proposed circuits for reducing power consumption, propagation delay, and area is evaluated at scaled supply voltages down to the subthreshold regime.

The paper is organized as follows. The operation of the proposed level converters is described in Section 2. The power consumption and the propagation delay characteristics of the level converters at the nominal process corner and under parameter variations are presented in Section 3. Finally, some conclusions are provided in Section 4.

2. LEVEL CONVERTERS
In this section various level conversion techniques are described. The issues related to the standard feedback-based level converters are discussed in Section 2.1. Three new level converters based on a multi-Vth CMOS technology are presented in Section 2.2.

2.1 Feedback-Based Level Converters
The conventional feedback-based level converters are discussed in this section. When a low swing signal directly drives a gate that is connected to a higher supply voltage, the pull-up network of the receiver cannot be fully turned off. A receiver driven by a low voltage swing signal therefore produces static dc current. In order to suppress this dc current, specialized voltage interface circuits are employed between a low voltage driver and a full voltage swing receiver [2], [4]–[10]. In the standard feedback-based voltage interface circuits, the pull-up network transistors are not directly driven by the low voltage swing signal provided by the driver. The operation of the pull-up network transistors is controlled by an internal feedback mechanism isolated from the low voltage swing input signal, thereby avoiding the formation of static dc current paths within the circuit. These traditional level converters, however, suffer from high short-circuit power and long propagation delay due to the typically slow response of the internal feedback circuitry that controls the operation of the pull-up transistors. Furthermore, the pull-down network

transistors in these circuits are driven by low voltage swing signals unlike the pull-up network transistors that receive higher gate overdrive voltages from the full-voltage swing feedback paths. Particularly, at very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to balance the strength of the pull-up and the pull-down networks.This causes further degradation in the speed and the power efficiency of the conventional level converters when utilized with very low input voltages.

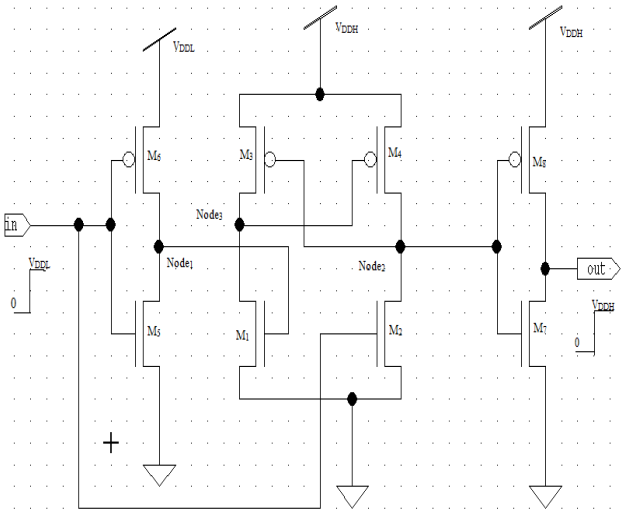


Figure 1. Standard level converter (LC1) presented in [2]. V_{DDL} is the lower supply voltage. V_{DDH} is the higher supply voltage.

The standard feedback-based level converter (LC1) [2] is shown in Figure 1. M_1 and M_2 experience a low gate overdrive (V_{DDL} − Vth) voltage during the operation of the circuit. M1 and M_2 and need to be sized larger to produce more current as compared to and, respectively, for functionality. The circuit operates as follows. When the input is at 0 V M_2 is turned off. $Node_1$ is charged to V_{DDL}. M_1 is turned on. $Node_3$ is discharged to 0 V turning M_4 on. $Node_2$ is charged to V_{DDH} turning M_3 off. The output is pulled down to 0 V.When the input transitions to V_{DDL}, M_2 is turned on. $Node_1$ is discharged, turning M_1 off. $Node_2$ is discharged, turning M_3 on.$Node_3$ is charged up to V_{DDH} turning M_4 off. The output transitions to V_{DDH}. A feedback loop, isolated from the input, controls the operation of M_3 and M_4 during both transitions of the output.

Due to the transitory contention between the pull-up and the pull-down networks and the large size of the nMOS transistors (M_1 and M_2), however, LC1 consumes significant short-circuit and dynamic switching power. To maintain functionality with the lower values of V_{DDL}, the sizes of M_1 and M_2 need to be further increased in order compensate for the gate overdrive degradation. The load seen by the previous stage (driver circuit) is therefore increased, thereby further degrading the speed and increasing the power consumption. Tapered buffers are required to drive and at very low voltages. These tapered buffers further increase the power consumption of LC1.

Another level converter (LC2) is presented in [4] for enhanced speed as compared to LC1. LC2 is shown in Figure 2. M_6 maintains the voltage of between V_{DDL} and V_{DDL}+ Vthn in order to enhance the current produced by M_1.The capacitor (C=1PF) stabilizes the voltage of $Node_3$ against the noise induced by the nearby switching events.

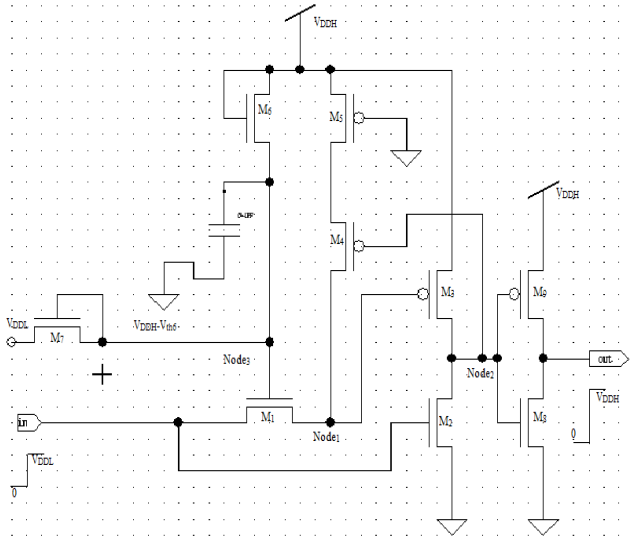


Figure 2. Level converter (LC2) presented in [4].

The circuit operates as follows. When the input is at 0 V, $Node_1$ is discharged throughM_1. M_3 is turned on.M_2 is turned off. Node2 is charged to V_{DDH}, turning M_4 off. The output is discharged to 0 V. When the input transitions to V_{DDL}, M_2 is turned on.$Node_1$ is initially charged to a voltage between V_{DDL}-Vthn and V_{DDL} through M_1. M_3 is not completely cutoff (weakly active). M_2 is sized to be stronger than M_3 for the circuit to function properly. Node2 is discharged, turning M4 on.$Node_1$ is charged all the way up to V_{DDH} , thereby eventually turning M_3 off. The output transitions to V_{DDH}. When the input switches from 0 V to V_{DDL} there is a direct current path from V_{DDH} to Gnd through the M_2–M_3 path. This direct current path exists until Node1 is charged to V_{DDH} through M4 and M5. Similarly, when the input switches from V_{DDL} to 0 V, there is a direct current path from V_{DDH} to Gnd through the M_5 –M_4 –M_1 path. This direct current path exists until node2 is pulled up to V_{DDH} and M_4 is turned off. LC2 therefore consumes significant short-circuit power, similar to LC1, during both low-to-high and high-to-low transitions of the output. Furthermore, when V_{DDL} is reduced, a significant increase in the size of is required for maintaining functionality. The load seen by the driver circuit therefore increases at lower V_{DDL}. Tapered buffers are required for driving LC2 at very low voltages. These tapered input drivers further increase the power consumption of LC2.

2.2 Multi-Vth Level Converters

Three new multi-Vth level converters are described in this section. Unlike the previously published level converters that rely on feedback, the proposed level converters employ a multi-Vth CMOS technology in order to eliminate the static dc current. The high threshold voltage pull-up network transistors in the new level converters are directly driven by the low-swing signals without producing a static dc current problem.

The first proposed level converter (PC1) is shown in Figure 3. PC1 is composed of two cascaded inverters with dual-Vth

transistors. The threshold voltage of is more negative (higher |Vth|) for avoiding static dc current in the first inverter when the input is at V_{DDL}. $|V_{th-M2}|$ is required to be higher than V_{DDH}-V_{DDL} for eliminating the static dc current. PC1 operates as follows. When the input is at 0 V, M_2 is turned on.M_1 is cutoff. Node1 is pulled up to V_{DDH}. The output is discharged to 0 V. When the input transitions to V_{DDL}, M_1 is turned on. M_2 is turned off since $V_{GS,\ M2} > V_{th,\ M2}$. $Node_1$ is discharged to 0 V. The output is charged to V_{DDH}.

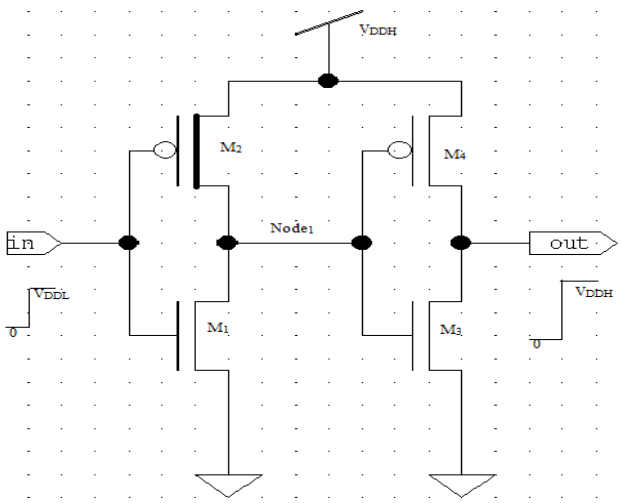


Figure 3. First proposed level converter (PC1). Thick line in the channel area indicates a high -Vth device.

PC1 has fewer transistors as compared LC1 and LC2. Furthermore, the elimination of the slow feedback circuitry reduces the short-circuit power of PC1 as compared to LC1 and LC2. For the lower values of V_{DDL}, the threshold voltage of M2 needs to be more negative (higher -|Vth|) in order to suppress the static dc current. Provided that a multi-Vth CMOS technology is available, no increase in the size of is required for achieving functionality at lower input voltages with the proposed circuit (unlike LC1 and LC2). Therefore, particularly for the very low values of V_{DDL}, PC1 consumes lower power, occupies significantly smaller area, and imposes a much smaller load capacitance on the input driver as compared to LC1 and LC2.

The circuit configurations of the second proposed level converter (PC2) for operation at different supply voltages are shown in Figure 4. $|V_{th-M2}|$ is required to be higher than V_{DDH}-V_{DDL} for eliminating the static dc current when the input is low (Node1 is at V_{DDL}). The peripheral circuitry composed of M3, M4 and C, shown in Fig. 4(a), is employed to maintain the voltage in the range of

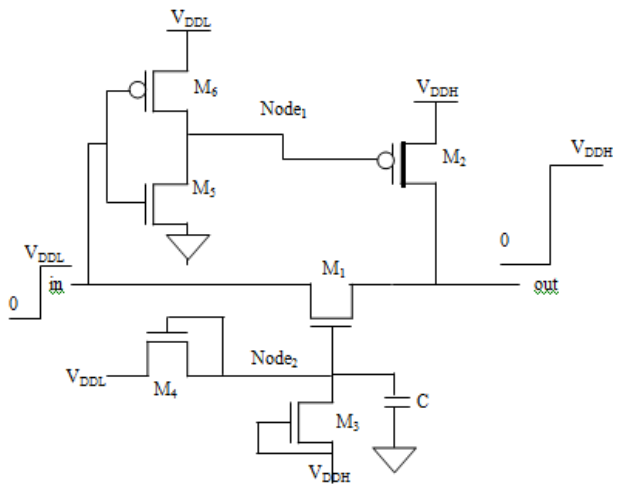
$$V_{DDL}<V_{Node2}<V_{DDL}+V_{th-M1} \quad (1)$$

in order to enhance the speed of charge transfer through M_1 while avoiding the formation of a static dc current path within the level converter. M_3 maintains the voltage of $Node_2$ at

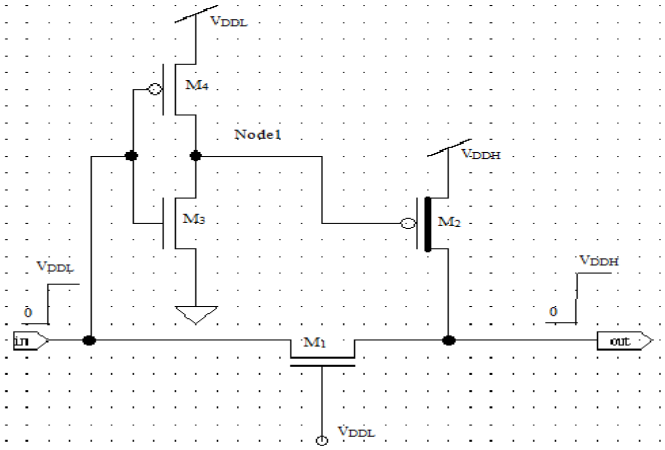
$$V_{Node2}=V_{DDH}-V_{th-M3} \quad (2)$$

provided that

$$V_{DDH}-V_{th-M3}<V_{DDL}+V_{th-M4} \quad (3)$$



(a)



(b)

Figure 4. Second proposed level converter (PC2). Thick line in the channel area indicates a high-Vth device. (a) Circuit configuration for $V_{DDL}$and V_{DDH} that satisfy both (1) and (3). (b) Circuit configuration for the supply voltages that do not satisfy either (1) or (3).

If (3) is satisfied, M_4 is maintained cutoff under normal operating conditions with no external noise coupling onto $Node_2$. The purpose of M_4 is to provide a discharge path for $Node_2$ if the voltage on temporarily exceeds $V_{DDL}+V_{th-M4}$ due to nearby switching events and crosstalk. The capacitor(C=1PF) stabilizes the voltage of against the noise induced by the nearby switching events. If, however, (3) is not satisfied for the very low values of V_{DDL}, a dc current path exists between V_{DDH} and V_{DDL} through M3 and M4. In order to avoid a static dc current path within the level converter M3, M4, and the capacitor C are eliminated and $Node_2$ is directly connected to V_{DDL} for the

voltages that do not satisfy (3), as shown in Fig. 4(b). Similarly, if (1) is not satisfied for certain values of V_{DDL} and V_{DDH}, Node2 is directly connected to V_{DDL}, eliminating the need for M3, M4 and C as shown in Fig. 4(b).

PC2 operates as follows. When the input is at 0 V, $Node_1$ is pulled high to V_{DDL} turning M_2 off (note that M_2 has a high-|Vth|). The output node is discharged to 0 V through the pass transistor M_1. When the input transitions to V_{DDL}, the output node is initially charged to V_{DDH} -V_{th-M1}-V_{th-M3} and V_{DDL}- V_{th-M1} through M_1 with the circuit configurations shown in Fig. 4(a) and (b), respectively. M_2 is turned on after the high-to-low propagation delay of the inverter (I_1). The output is pulled high all the way up to V_{DDH} through M_2. M_1 is turned off isolating the two power supplies. Both M_1 and M_2 assist the output low-to-high transition, thereby eliminating the contention current and enhancing the low-to-high propagation speed. The small transistor count and the elimination of the feedback reduce the power consumption of the proposed level converter as compared to LC1 and LC2.Furthermore, the speed of PC2 is enhanced due to the shorter input-to-output signal propagation path (composed of only one pass transistor) and the elimination of the contention current during the output low-to-high transition.

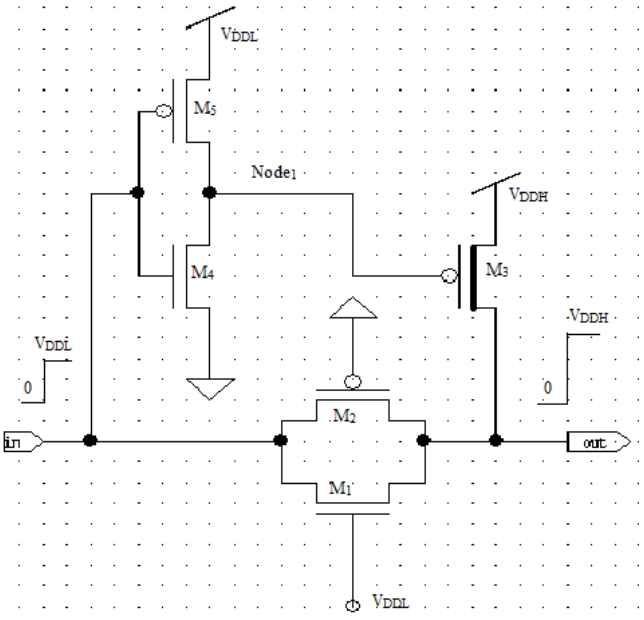


Figure 5. Third proposed level converter (PC3).Thick line in the channel area indicates high-Vth device.

PC3 operates as follows. When the input is at 0 V, $Node_1$ is pulled high to V_{DDL} turning M_3 off (note that M_3 has a high-|Vth|). The output node is discharged to 0 V. When the input transitions to V_{DDL}, the output is charged V_{DDH} through the transmission gate comprising of M_1 and M_2.

3. SPEED AND POWER CONSUMPTION CHARACTERISTICS

In this section, the three new level converters are compared to the previously published standard feedback-based level converters for average power consumption and propagation delay.

Table 1. Average Power consumption (P), Average Propagation Delay (D), Rise time (t_r), Fall time (t_f) of the Level converters

Level Converter	Power Consumption P (Watts)	Delay D (Sec)	Rise time t_r (Sec)	Fall time t_f (Sec)
LC1	1.038n	3.77n	56.684p	232.54p
LC2	462.8066n	1.60n	55.28p	64.4p
PC1	670.4075p	0.179p	285.2p	220.94p
PC2 (a)	461.985n	121.03p	2.27ns	2.31ns
PC2 (b)	121.57p	148.23p	2.08n	1.8n
PC3	139.63p	74.02p	3.60n	3.58n

4. CONCLUSION

In this paper, three novel level converters based on a multi-Vth CMOS technology are proposed. Unlike the standard level converters based on feedback, the new circuits employ multi-Vth transistors in order to suppress the dc current paths in CMOS gates driven by low-swing input signals. Pass transistors are good for passing either a high signal or a low signal causes unequal rise and fall delays. Using transmission gate in level converters we can get equal rise and fall time. The proposed circuits maintain higher speed and lower power consumption characteristics as compared to the conventional feedback-based level converters for a wide range of available threshold voltages with different multi-Vth CMOS technologies.

5. ACKNOWLEDGMENT

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