Effect of underlap on 30 nm Gate Length FinFET based LNA using TCAD Simulations

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ABSTRACT
The effect of gate – drain/source underlap (L_{un}) on a narrow band LNA performance has been studied , in 30 nm FinFET using device and mixed mode simulations. Studies are done by maintaining and not maintaining the leakage current (I_{off}) of the various devices. LNA circuit with two transistors in a cascode arrangement is constructed and the input impedance, gain and noise-figure have been used as performance metrics. To get the better noise performance and gain, L_{un} in the range of 3-5 nm is recommended.

Keywords
FinFET; LNA; TCAD; Underlap

1. INTRODUCTION
Scaling of CMOS technology not only promises gigabit integration, gigahertz clock rate, and systems on a chip, but also arouses great expectations for CMOS RF circuits in gigahertz range [1]. Drain induced barrier lowering (DIBL) and Short channel effects (SCE) are becoming the fundamental limiting factors in scaling of a single gate planar CMOS transistor. FinFETs are emerging as a potential alternative to MOSFETs due to their quasi planar structure and compatibility with CMOS technology. FinFET, a recently reported novel double-gate structure, the Si fin forms the channel and gate wraps around the fin. The Si fin has insulator on top and gate on either side, current flows parallel to the device surface.

A low noise amplifier (LNA) is a key component in RF front-end receivers which poses a major challenge in terms of meeting high gain and low noise figure at low power supply voltages. In this paper, a FinFET based LNA has been designed and the effect of underlap (L_{un}) on LNA parameters such as input impedance (Z_{IN}), gain (S_{21}) and noise figure (NF) have been studied. This paper presents a LNA design using 30 nm FinFET and the effect of underlap on LNA performance. In the next section, TCAD simulator and the simulation methodology have been discussed. Simulation results are discussed in the section 3. Finally, section 4 gives the conclusion.

2. SIMULATOR AND SIMULATION METHODOLOGIES

2.1 Simulator
Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- Sentaurus structure editor (SDE): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations
- Inspect and Tecplot: To view the results.

Mixed mode simulation facility of SDEVICE is used to investigate the performance of LNA. The physics section of SDEVICE includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. Noise models such as diffusion noise, monopolar generation-recombination noise, bulk flicker noise are included while doing noise simulations. The structure generated from SDE is shown in Fig. 1. Doping and mesh information can also be observed in Fig. 1. Fig. 2 shows the schematic diagram of the device. The various parameters of the device can be seen in Fig. 2. Table 1 gives the dimensions of the typical device used in this study.

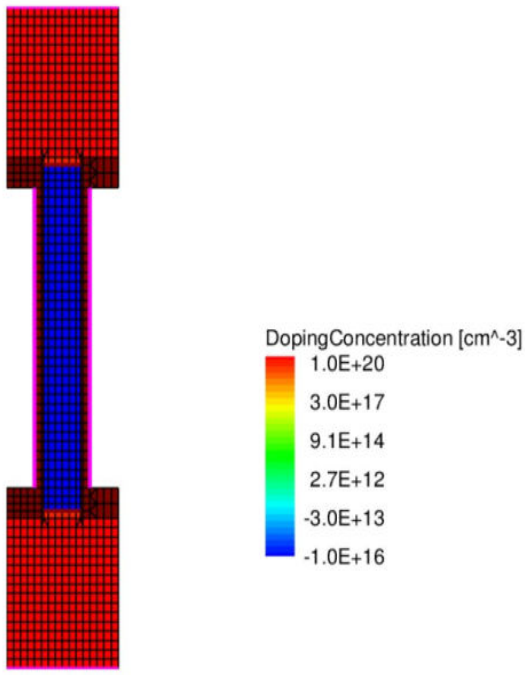

Figure 1. Structure generated from TCAD

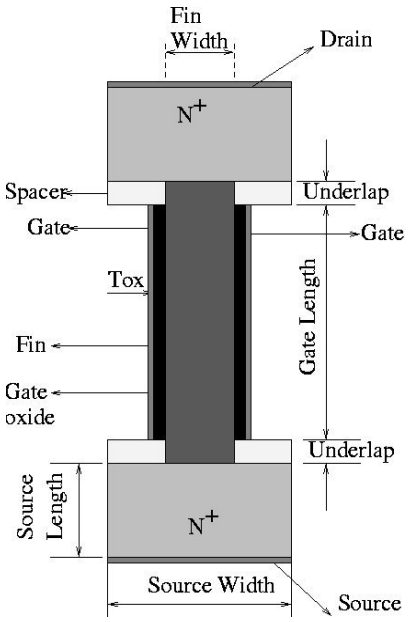

Figure 2. Schematic view of Dual-Gate FinFET

Table 1. Typical device dimensions

Parameters	Typical Value
Gate Length	30 nm
Fin Width	5 nm
Source width	15 nm
Source length	15 nm
Gate oxide thickness	2 nm

2.2 Simulation methodologies

The LNA circuit used in this study is shown in Fig. 3. Generally, a common source LNA is used with a source degeneration inductor to get the impedance match, especially to get the real part of input impedance. But, this circuit does not use any source inductor. Instead, it exploits the non-quasi-static (NQS) effects or the channel resistance which arises due to finite charging time of the channel carriers to get the impedance match [2]. An input impedance of 50 Ω, purely resistive, is desired for LNA. The imaginary part i.e. the capacitive part of the input impedance is cancelled at the given frequency, by connecting an appropriate inductor at the gate (L_g). SDEVICE simulator is used for mixed mode simulation of LNA circuit (Fig. 3). Transistors M1 and M2 are simulated at the device level. Other elements are simulated using the compact models at the circuit level. M1 and M2 are identical transistors. Inductors L_g and L_o, are used with their series resistance incorporated, and a quality factor of 5 is assumed. Resistances associated with the inductors are given by the following familiar expression,

$$R = \frac{2\pi f .inductor\_value}{quality\_factor} \quad (1)$$

The circuit is operated at the supply voltage of V_{dd} = 1 V, V_{gs} of M1 = 0.5 V and L_o = 1.5nH. The operating frequency (f) of LNA is taken as 10 GHz.

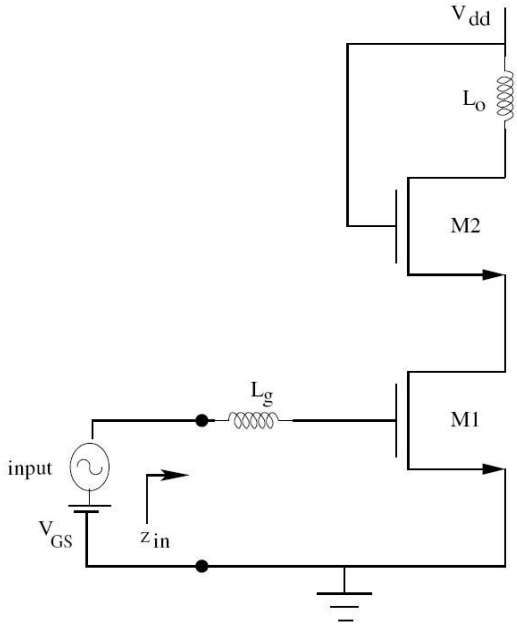

Figure 3. LNA circuit used in this study

The standard AC simulations are done over a range of frequencies. SDEVICE outputs are in the form of admittance and capacitance matrices. They are converted to **S** parameter and $\mathbf{S_{21}}$ is taken as gain of LNA.

Noise simulation in SDEVICE is standard AC simulation with noise models included in the physics section. Noise-figure (NF) calculation is done by assuming a signal source resistance (purely resistive) of 50 Ω.

For a two port network NF is defined as [3], [4],

$$NF = 1 + \frac{1}{S_I^S}\left(S_I^{gg} + |\alpha|^2 S_I^{dd} - 2\,\mathrm{Re}(\alpha S_I^{dg})\right\} \quad (2)$$

With

$$\alpha = \frac{Y_S + Y_{11}}{Y_{21}} \quad (3)$$

Where S_I^S is the current noise spectrum of the noisy source admittance and is given by,

$$S_I^S = 4k_B T\,\mathrm{Re}(Y_S) \quad (4)$$

S_I^{gg} and S_I^{dd} are the current noise spectrums, at the gate and drain terminals respectively, S_I^{dg} is the cross-correlation noise spectra between the drain and gate terminals, Y_{11} and Y_{21} are the respective admittance (Y) parameters.

When the underlap is changed, the effect is reflected in the device level (I_{off}, I_{on}, V_{th}, g_m, f_t, etc.) as well as in the circuit level (LNA performance metrics such as input impedance, gain, and noise figure). Therefore, two case studies are constructed and LNA performance is studied.

- Case 1: Underlap is changed and I_{off} not maintained
- Case 2: Underlap is changed and I_{off} maintained

3. RESULTS AND DISCUSSION

Fig. 4 shows the variation in the leakage current (I_{off}) and drain current (I_{on}) of the 30 nm FinFET with the different L_{un} values. As L_{un} is increased, the series resistance associated with the channel increases thereby reducing I_{off} and I_{on} which can be observed in Fig. 4.

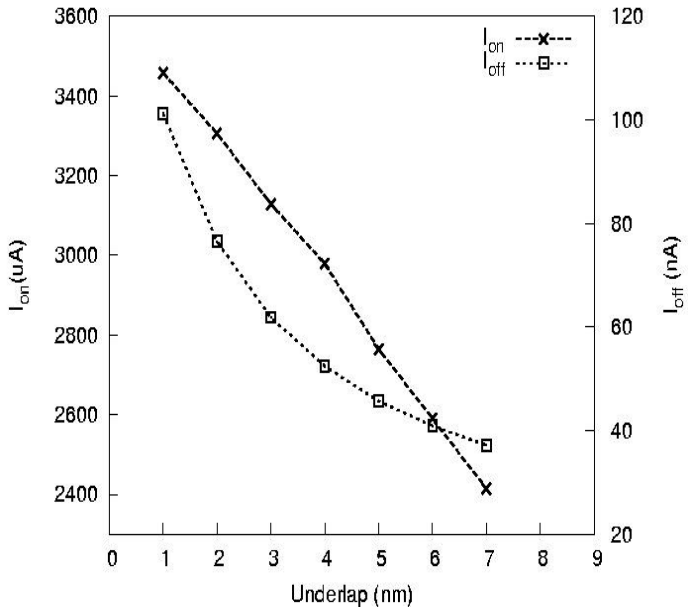

Figure 4. The effect of L_{un} on I_{off} and I_{on}

Using 0.5 nm as L_{un} and other parameter as shown in Table 1, a FinFET is generated. Using this device, LNA simulation is done in SDEVICE simulator and the mixed mode simulation approach is followed. Appropriate values of gate inductor and transistor width provide an input impedance of 50 Ω (purely real). After input impedance matching, the gain and NF are extracted (S_{21}=9.21 dB, NF=1.977 dB). FinFETs with different L_{un} are created which is followed by LNA simulations. Figure 5 shows the input impedance, both real and imaginary, as a function of L_{un}. It can be seen from Fig. 5 that both real and imaginary part of the input impedance increases when L_{un} increases. The input impedance of LNA circuit shown in Fig. 3 is given by,

$$Z_{in} = R_{Lg} + R_g + r_i \tag{5}$$

where R_{Lg} is the resistance due to gate inductor, R_g is the intrinsic gate resistance, and r_i is due to NQS effect. If we assume proper layout technique have been adopted R_g can be ignored. Since r_i increases with L_{un} [5], the real part of the input impedance increases with L_{un}. C_{geff} in DGMOS can be expressed as [6],

$$C_{geff} = Series(C_{ox}, C_{si}) \,||\, C_{ov} \,||\, C_{fringing} \tag{6}$$

where C_{ox} is the oxide capacitance, C_{si} is the silicon body capacitance, C_{ov} is the gate to source/drain overlap capacitance and $C_{fringing}$ is the fringing capacitance. In our device C_{ov}= 0,

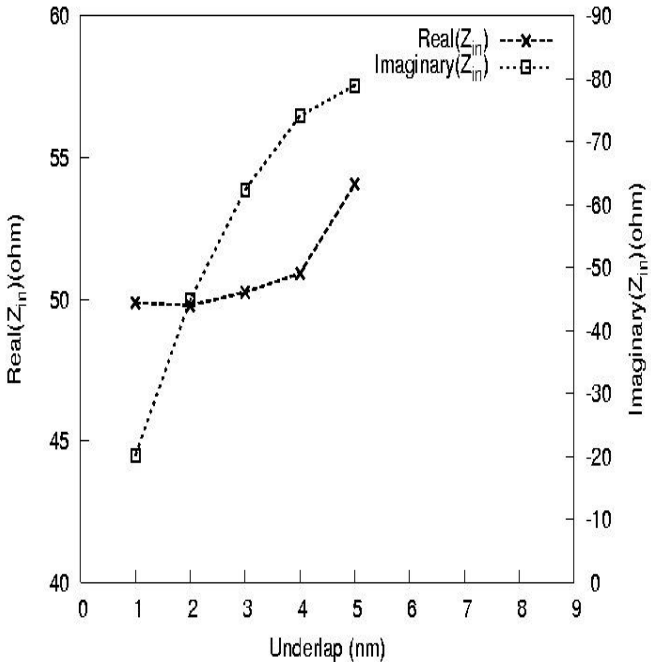

Figure 5. Real and Imaginary part of input impedance versus Underlap of the device

because no overlap exists between gate and source/drain. $C_{fringing}$ is given by [7],

$$C_{fringing} = \frac{k\varepsilon_{di}W}{\pi} \ln \frac{\pi W}{\sqrt{L_{un}^2 + T_{ox}^2}} e^{-\left|\frac{L_{un}^2 - T_{ox}^2}{L_{un}^2 + T_{ox}^2}\right|} \tag{7}$$

For the given transistor width (W), as per (7), when L_{un} increases, $C_{fringing}$ decreases, which in turn decreases the C_{geff} with the increased capacitive reactance. So the imaginary part of the input impedance increases with L_{un}.

Case 1

It has been seen that the change in L_{un} affects the input impedance. When L_{un} is changed the input impedance can be matched by adjusting the gate inductor and the width of the transistor. Case 1

focuses on this procedure. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real, are shown in Table 2. Since real part of the input impedance increases with L_{un} (Fig. 5), we need larger transistor widths to achieve 50 Ω, real part. Again it may be recollected from Fig. 5 that L_{un} increases the input capacitive reactance (i.e. imaginary part of input impedance) thereby demanding higher gate inductor values. But it can be noticed from Table 2 that after 4 nm of L_{un} the required gate inductor value decreases. For higher L_{un} s, larger transistor widths are needed to make real part of the input impedance equal to 50 Ω. But this procedure at some point makes C_{geff} to go up i.e. we need smaller gate inductors to cancel out the capacitive reactance. In our simulation, this happens when L_{un}=4 nm (refer Table 2).

Table 2. Values of L_{un}, L_g, f_t, Width and their respective Gain, Noise figure (I_{off} not maintained)

L_{un} (nm)	Gate inductor (nH)	f_t (GHz)	Width of the transistor (µm)	Gain (S_{21}) (dB)	NF (dB)
0.5	1.35	735.759	16	9.21	1.977
1	1.55	815.095	17	9.777	1.914
2	1.75	881.399	19	10.737	1.819
3	1.9	889.733	20	11.02	1.726
4	1.95	888.382	21	11.243	1.675
5	1.9	854.405	22	10.889	1.657
6	1.7	829.335	24	10.625	1.708
7	1.55	801.741	25	9.730	1.738

From Fig. 6 it is observed that the gain of the LNA is going through a peak i.e. the gain increases and then decreases with respect to L_{un}. A maximum gain value of 11.243 dB occurs at L_{un}= 4nm. On one hand, the increased transistor width used with increased L_{un}, enhances g_m and thereby the gain. But on another hand increased L_{un} increases the series resistance and thereby degrades g_m at some point which in turn lowers the gain. In essence, for lower values of L_{un}, increase in the transistor width is responsible for increase in g_m and the decrease in $C_{fringing}$ is responsible for the decrease in C_{geff}. And at higher values of L_{un}, increase in the series resistance is responsible for g_m degradation and the increase in the transistor width increases $C_{fringing}$ which is responsible for the increase in C_{geff}. From Fig. 6 it can be noticed that NF travels through a minima when L_{un} is varied. Around L_{un}=4 nm a minimum value of NF is achieved. Let us consider the input stage of Fig. 3. We have a common source amplifier, with an inductor and resistor (includes the parasitic resistance of the inductor) at the gate. Noise-Figure of this stage alone is given by [8],

$$NF = 1 + \left(\frac{f_o}{f_t}\right)K \qquad (8)$$

where f_o – resonant frequency, f_t – unity gain frequency, and K is noise factor scaling coefficient, and depends on the resonant frequency, quality factor of the inductor, ratio g_m / g_{d0} (g_m is transconductance of the FinFET, g_{d0} is output conductance of the FinFET at zero drain bias) and process specifications.

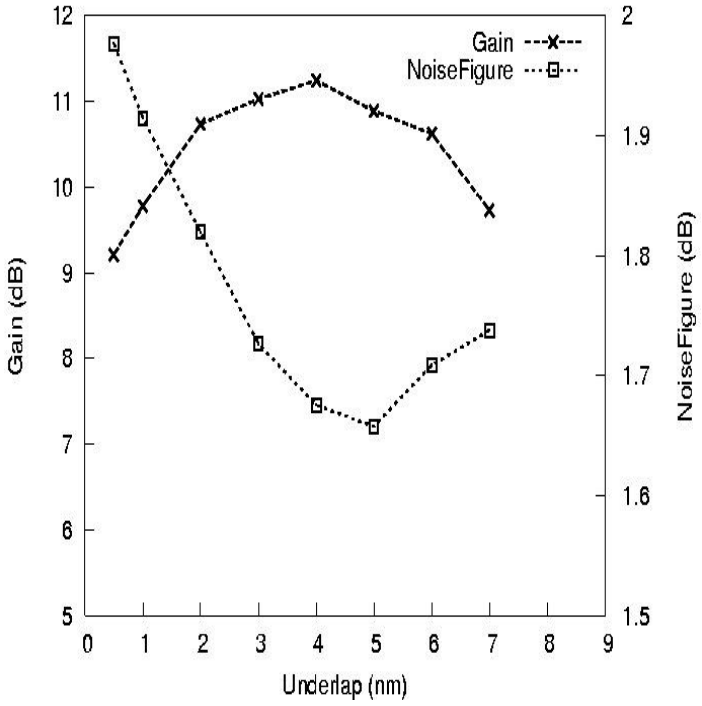

Figure 6.Gain (dB) and Noise Figure (dB) of LNA after getting a 50 Ω input impedance match at 10 GHz, for different underlaps

Equation (8) tells that NF is decided by K and f_t once we fix the frequency of operation or resonant frequency. As already discussed g_m increases where as C_{geff} decreases for L_{un} values up to 4nm, after which they reverse the trend. It is well known that f_t is directly proportional to g_m and inversely proportional to C_{geff}. Therefore, f_t increases up to L_{un}=4 nm and then starts decreasing (refer Table 2). This causes NF to decrease and then increase when L_{un} is increased.

Case 2

When L_{un} is varied it not only affects the input impedance of LNA but also affects the device leakage (I_{off}). When L_{un} is increased both I_{off} and I_{on} decrease. To have a fair comparison between the devices with different L_{un}s, a constant I_{off} constraint can be superimposed. When L_{un} of the device is varied I_{off} is maintained around 50 nA and the gate electrode work function (WF) is adjusted to achieve this constraint. Once again, when L_{un} is changed the input impedance matching was achieved by adjusting the gate inductor and transistor width. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real are shown in Table 3. It also gives WF, f_t of the various devices, and their respective gain and noise figure values.

Table 3. Values of L_{un}, WF, f_t, L_g, Width and their respective Gain, Noise figure (I_{off} maintained)

L_{un} (nm)	WF (eV)	f_t (GHz)	Gate inductor (L_g) (nH)	Width of the transistor (µm)	Gain (S_{21}) (dB)	NF (dB)
0.5	4.336	737.26	1.45	16	9.39	1.102
1	4.334	815.18	1.65	17	9.974	1.045
2	4.324	866.09	1.9	19	11.04	0.983
3	4.317	866.21	2.05	20	11.39	0.978
4	4.312	840.50	2.05	22	12.10	0.962
5	4.307	812.30	2.05	23	11.83	0.993
6	4.304	773.54	1.95	24	11.22	1.026
7	4.301	737.29	1.75	26	10.60	1.071

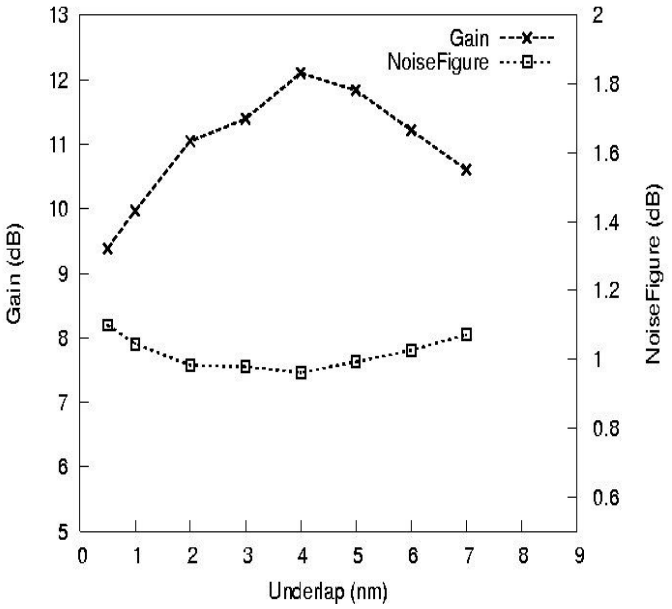

Figure 7. Gain(dB) and Noise Figure(dB) of LNA after getting a 50Ω input impedance match at 10 GHz, for different underlaps with I_{off} = 50 nA (maintained through gate work function)

Fig. 7 depicts the gain and NF against L_{un} and it can be noticed from Fig. 7 that both the gain and NF have some optimum L_{un} i.e. around L_{un}=4 nm, we get 12.1 dB gain and 0.96 dB NF. The behavior of the gain and NF shown in Fig. 7 is same as Fig. 6 of case 1. It can be reasoned out in the same manner as in case 1.

4. CONCLUSION

In this paper, we have investigated the effect of L_{un} on gain and NF of a 10 GHz, narrow band LNA using TCAD simulations. Changing L_{un} was followed by two philosophies, not maintaining I_{off} and maintaining I_{off}. When I_{off} was not maintained, a maximum gain of 11.243 dB was achieved at L_{un}= 4 nm and a minimum NF of 1.657 dB was achieved at L_{un}=5 nm. When I_{off} was maintained around 50 nA, a maximum gain of 12.105 dB and a minimum NF of 0.962 dB was achieved at L_{un}= 4 nm. L_{un} in the range of 3-5nm will give optimum gain and NF for this LNA design.

5. ACKNOWLEDGEMENT

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