

Simulation & Design Two New Full Adder Cells Based on Inverse Majority Gate in Subthreshold Region by Various CMOS Technologies

Manijeh alizadeh
Messgar
Scientific Association of
Electrical&Electronic
Engineering, Islamic Azad
University Central Tehran
Branch, Tehran,Iran

Behjat forouzandeh
ECE, university of Tehran,
Tehran,Iran

Reza Sabbaghi-
nadooshan
Islamic Azad University,
Central Tehran Branch
Tehran,Iran

ABSTRACT

This paper presents two new 1-bit full adder cells operating in subthreshold region with 65nm, 90nm and 0.18um technologies. Circuits designed in this region usually consume less power. Inverse Majority Gate (IMG) together with NAND/NOR were used as the main computational building blocks. A modification was done to optimize W/L ratios with different supply voltages. We used W/L ratios for all the PMOS transistors 1.5 times the ratio of W/L for all NMOS transistors. Results are compared with a previously reported minority-3 based full adder; the results involve better performance in terms of power, delay and PDP.

General Terms: VLSI DESIGN

Keywords: VLSI, Subthreshold, full adder, inverse majority gate.

1. INTRODUCTION

In this paper we proposed two new structures for 1-bit full adder cell based on the sub threshold perceptron introduced in [1],[2]. These structures have been simulated by various CMOS technologies and their results are compared with simulation results of minority-3 based 1-bit full adder [3], [4] (Min3 IJCNN Based on the dynamically reconfigurable "IJCNN"-element [1],[5] that configured as a minority-3 gate by biasing the wells of the element). The input waveforms contain all the possible transitions from one input combination to another (56 patterns) [6], [7]. The accuracy and characteristics of the structures have been investigated and reported in the following sections. The paper is organized as follows.

In section 2, behavior of transistors in sub threshold region is described in brief. The idea of using substrate terminal voltage to control resistance of transistors in sub threshold region is introduced in this section. Using this intuition, a block of 6 transistors (IJCNN [3]) proposed in [3], [4], [8] has been used to design three input gates of inverse majority, NAND and NOR and the output wave forms derived from Hspice simulations are brought in Section 3. In section 4, it is considered the minority-3 based 1-bit full adder mentioned in [3]. Majority not gates are

replaced with block of 6 transistors (Min3 IJCNN). In section 5, the proposed full adder structures are drawn. Study of their characteristics is explained in section 6. Section 7 is dedicated to summary and conclusion.

2. DISCUSSION OF TRANSISTORS IN SUB THRESHOLD REGION

For an NMOS transistor operating in sub threshold region, the current between drain and source is expressed as in equation (1) [7].

$$I_{ds,n} = I_0 \exp\left\{\frac{\kappa V_{gs}}{V_t}\right\} \exp\left\{(1-\kappa)\frac{V_{bs}}{V_t}\right\} \left[1 - \exp\left\{\frac{-V_{ds}}{V_t}\right\} + \frac{V_{ds}}{V_0}\right]$$

(1) Here, I_0 is a constant and shows the current between drain and source while the transistor is in zero bias and it is affected by the length and width value of the transistor. V_0 is the Early voltage and is proportional to L. κ is a coefficient with which the channel current is related to the gate voltage and is approximately variable between 0.7 to 0.75 V. V_t is the thermal voltage and is equal to $\frac{kT}{q}$. Equation 1 shows that the substrate

and the gate voltages have the capability to control $I_{ds,n}$ [8].

3. DESIGN OF INVERSE MAJORITY, NAND AND NOR GATES IN SUB THRESHOLD REGION

Figure 1 shows a block of 6 transistors, all are working in sub threshold region. In order to keep the transistors in sub this region, it is required that Vdd be less than |Vth| of both NMOS and PMOS. In other words, considering the worse case ,that is the input signal has the value of Vdd, $V_{gs \ xNMOS} = V_x = V_{dd}$.Note that $V_{gs \ xNMOS}$ is the voltage across gate and source of the transistor with its gate connected to input x. To keep it in sub threshold region it is required,

$V_{gs \text{ xNMOS}} < V_{th}$. Since $V_{gs \text{ xNMOS}} = V_x = V_{dd}$, this leads to $V_{dd} < V_{th}$. According to equation 1, an increase in substrate voltage causes an increase in I_{ds} of NMOS transistors as well as a decrease in I_{ds} of PMOS transistors. As mentioned earlier, the conductivity of a transistor is related to I_{ds} , thus the resistance of transistor has an inverse relation with I_{ds} .

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \quad (4)$$

Here, γ denotes the body effect coefficient, and V_{SB} is the source-bulk potential difference. Φ_F is given by $\frac{kT}{q} \ln(\frac{N_{sub}}{n_i})$ where N_{sub} is the doping concentration of the substrate. Equation (4) [9] shows the relation between the threshold voltage and substrate terminal voltage. Increasing the threshold voltage of a PMOS by an increase in substrate terminal voltage causes an increase in the resistance of PMOS. In another point of view, as the transistor goes toward being off, it shows more resistance. In figure 2(a) [1], [8] regarding to V_{gs} and V_{bs} values are determined resistor values and in figure 2(b) [4], resistors with greater value are depicted bigger in size. Transistors making the nonlinear resistive network determine the output voltage [8]. Resistors with greater value represent the transistors which are further deep toward being off. Resistors with smaller sizes represent transistors with smaller $|V_{th}|$, which are about to become on, still being in sub threshold region because of power considers. As shown in figure 2, each transistor is considered as a four terminal device, resistance of which is controlled by its gate and substrate terminal voltages. The complex of 6 such resistors, producing a voltage divider, determines the output voltage as depicted in figure 2. A complete description of this block is found in [8]. In order to implement the three input gates of inverse majority, NAND and NOR functions, we set the substrate voltage at 0, -Vdd and Vdd respectively. These blocks have been designed and simulated by HSpice using the 65nm standard CMOS technology at supply voltage of 0.2V and with switching frequency of 6.66 MHz. We used W/L ratios for all the PMOS transistors 1.5 times the ratio of W/L for all NMOS transistors. The output signals derived from the simulations are brought in figure 3.

4. MINORITY-3 BASED 1-BIT FULL ADDER

Minority-3 based 1-bit full adder [4], [5] is depicted in figure 4. Majority not gates are replaced with block of 6 transistors. A load capacitor of 60fF (is equaled with $10 \cdot C_{gs}$) was put at the output.

5. DESIGN OF TWO 1-BIT FULL ADDERS IN SUB THRESHOLD

5.1 Proposed Design 1

The functionality of the first proposed 1-bit Full Adder with A, B and Cin (input carry) inputs, and Sum and Cout (output carry) outputs, can be described by equation (5) and table 1. The primary design of the first proposed 1-bit full adder is depicted in figure 5(a). Substituting the designed inverse majority, NAND and NOR blocks from section 3, we reach to the new sub threshold full adder. A load capacitor of 20fF (is equaled with $10 \cdot C_{gs}$) was put at the output. The complete scheme is depicted in figure 5(b).

$$\text{Cout} = \text{majority}(A,B,\text{Cin}) \quad (5)$$

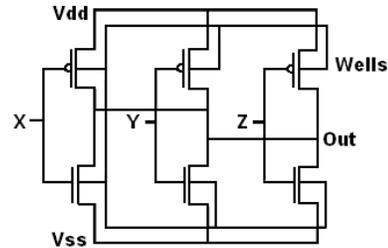


Figure 1. Block of 6 transistors (IJCNN) used to implement inverse majority, NAND, NOR gates in sub threshold region

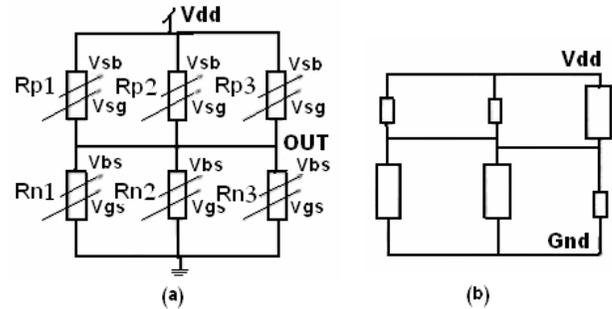


Figure 2. Block of figure 1, the inputs x and y are zero and the input z is vdd

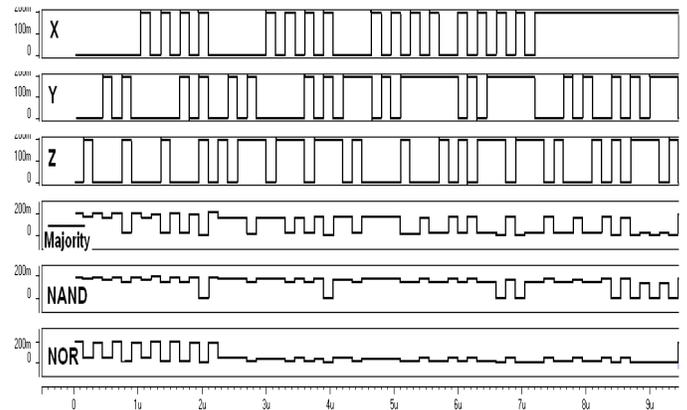


Figure 3. The inputs x, y and z and the outputs inverse majority, NAND and NOR. (Vdd=0.2, f=6.66 MHZ)

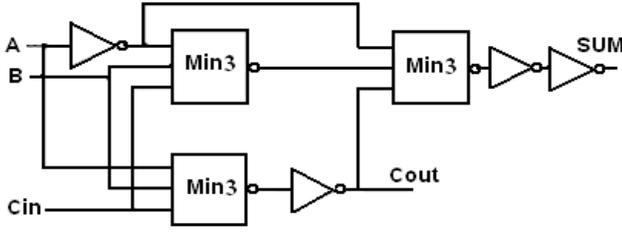


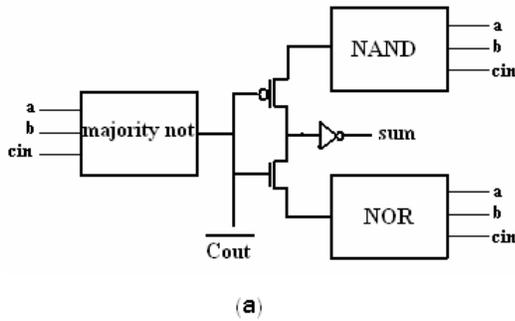
Figure 4. (a) Minority-3 based 1-bit full adder (Min3 IJCNN)

Table 1: Functionality of the first proposed 1-bit Full Adder

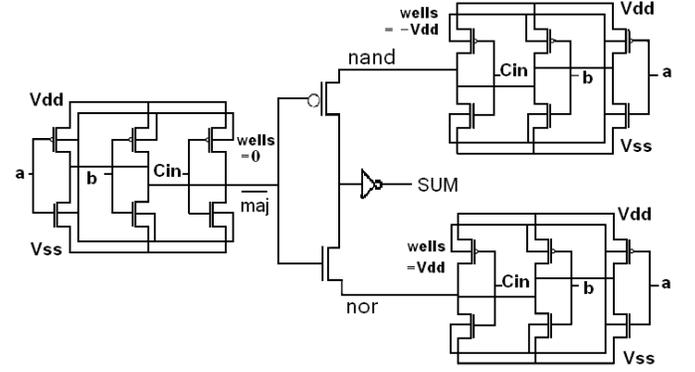
A	B	Cin	Majority not	NAND	NOR	Sum not
0	0	0	1	1	1	1
0	0	1	1	1	0	0
0	1	0	1	1	0	0
0	1	1	0	1	0	1
1	0	0	1	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	0	0	0	0

5.2 Proposed Design 2

The functionality of the second proposed 1-bit Full Adder with A, B and Cin (input carry) inputs, and Sum and Cout (output carry) outputs, can be described by equation (6) and (7) [10]. The second proposed primary design of 1-bit full adder is depicted in figure 6(a). The first block is a three input inverse majority gate and the second block is a five input one. It should be noticed that the inverse majority of inputs, a, b, and Cin is \overline{cout} . \overline{sum} is the majority of five inputs, a, b, Cin and two \overline{cout} s. The three input inverse majority gate could be implemented by the block of figure 1, as done in the first design. While the five input one could simply be implemented by adding two more paralleled inverters to the block of figure 1, making it a ten transistor structure. The complete scheme of the second 1-bit Full adder is depicted in figure 6(b). A load capacitor of 1fF (is equaled with $10 \cdot C_{gs}$) was put at the output.



(a)



(b)

Figure 5. (a) The first proposed 1-bit Full Adder. (b) A complete scheme

$$Cout = majority(A, B, Cin) \quad (6)$$

$$sum = Majority(A, B, Cin, \overline{Cout}, \overline{Cout}) \quad (7)$$

$$\overline{sum} = Majority not(A, B, Cin, \overline{Cout}, \overline{Cout})$$

6. SIMULATION RESULTS

The two new structures and minority-3 based 1-bit full adder, have been designed and simulated by Hspice in 65nm, 90nm and 0.18um standard CMOS technologies at three different values for supply voltage. The results have been compared with each others. We simulated all full adder cells at various frequencies ranging from 33.3 Hz to 33.3 MHz. Values of 0.25V, 0.2V, and 0.18V were chosen for Vdd. We used the same W/L ratios for all NMOS transistors. Values of W/L for PMOS transistors were always kept 1.5 times those of the NMOS transistors. The average power consumption of the simulated circuits is calculated by the following equation [11], [12]:

$$P_{avg} = P_{dynamic} + P_{short\ circuit} + P_{static} \quad (8)$$

$$= V_{DD} \cdot f_{clk} \cdot \sum_i (V_{i\ swing} \cdot C_{i\ load} \cdot \alpha_i) + V_{DD} \cdot \sum_i I_{i\ sc} + V_{DD} \cdot I_l$$

$P_{dynamic}$ denotes the switching component of power where, Vdd is the power supply voltage; f_{clk} is the system clock frequency, and V_{swing} is the voltage swing of the output, C_{load} is the output load capacitance at node i, and α_i is the transmission activity factor at node i. $P_{short-circuit}$ represent the short-circuit power, which results from I_{isc} following from power supply to ground at node i. P_{static} denotes the leakage power, which is

derived from leakage current I_l which is due to reverse-biased junction leakage current and subthreshold leakage current. The delay of cells has been measured from the moment that the inputs reach 50% of the supply voltage level to the moment that the latest of the Sum and Cout signals reach the same voltage level. All transitions from one input to another (56 patterns) have been checked and the delay has been measured for each transition. The maximum has been reported as the delay of each cell. Finally, for general comparison, the power-delay product (PDP) was calculated by following equation [10]:

$$PDP = \text{Maximum Delay} * \text{Average Power} \quad (9)$$

The results are reported in different diagrams. Figure 7 represent diagrams of power, propagation delay and PDP for minority-3 based 1-bit full adder, design 1 and design 2 in 65nm technology. This figure shows that design 2 has less delay, less power consumption and PDP than minority-3 based 1-bit full adder and design 1 for range V_{dd} s, 0.18, 0.2 and 0.25v. Values for power, delay and PDP in 65nm technology are reported in table 2. Figure 8 shows that diagrams of power, propagation delay and PDP for minority-3 based 1-bit full adder, design 1 and design 2 in 90nm technology. This figure represent that design 2 has minimum delay, minimum power consumption and PDP, design 1 in range 0.18 to 0.2v for V_{dd} , has less delay and in range 0.18 to 0.25v for V_{dd} , has less power consumption and PDP than minority-3 based 1-bit full adder. Values for power, delay and PDP in 90nm technology are reported in table 3. Figure 9 represent diagrams of power, propagation delay and PDP for minority-3 based 1-bit full adder, design 1 and design 2 in 0.18um technology. This figure shows that design 2 for range V_{dd} s, 0.18, 0.2 and 0.25v has minimum delay, power consumption and PDP, design 1 in range 0.18 to 0.25v for V_{dd} has less power consumption and in range 0.18 to 0.2v for V_{dd} has less PDP than minority-3 based 1-bit full adder. Values for power, delay and PDP in 0.18um technology are reported in table 4. Figure 10 shows diagrams of power, propagation delay and PDP for minority-3 based 1-bit full adder in all of three technologies. This figure shows that increasing of length channel causes the power consumption and PDP to decrease, while it causes the propagation delay to increase. Therefore in 0.18um technology, minority-3 based 1-bit full adder has less power, less PDP and more delay than 65nm and 90nm technology. Figure 11 shows diagrams of power, propagation delay and PDP for design 1 in all of three technologies. This figure shows that in 0.18um technology, design 1 has minimum power, in 90nm technology has minimum PDP and in 65nm technology has minimum delay. Figure 12 shows diagrams of power, propagation delay and PDP for design 2 in all of three technologies. Diagrams of this figure show that in 0.18um technology, design 2 has minimum power, in 90nm technology has minimum PDP and in 65nm technology has minimum delay. Therefore increasing of length channel in design 2 causes the power consumption to decrease and the propagation delay to increase.

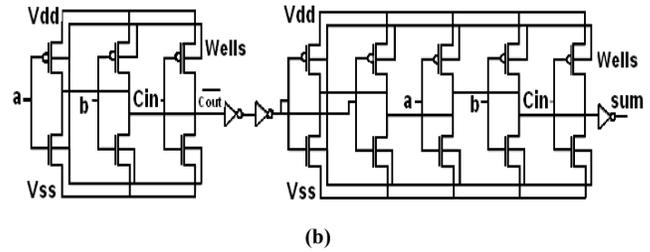


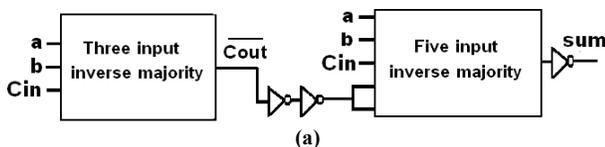
Figure 6. (a) The second proposed 1-bit full adder. (b) A complete scheme

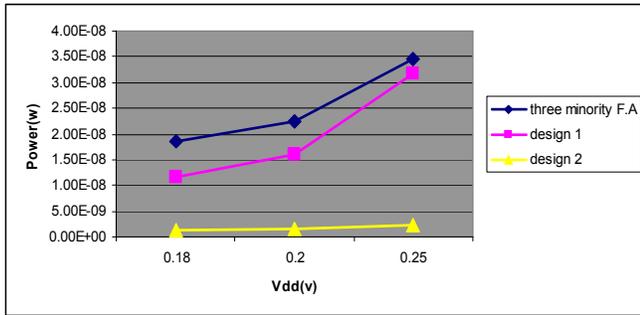
Table 2: values for power, delay and PDP in 65nm technology

Supply voltage(v)	0.18	0.2	0.25
Power(*e-8 w)			
Minority-3 based 1-bit F.A	1.87	2.24	3.45
Design1	1.15	1.59	3.17
Design2	0.124	0.151	0.244
Delay(*e-8 s)			
Minority-3 based 1-bit F.A	4.36	2.70	1.07
Design1	2.74	2.33	2.38
Design2	3.15	2.03	0.826
PDP(*e-16 J)			
Minority-3 based 1-bit F.A	8.15	6.05	3.69
Design1	3.15	3.70	7.54
Design2	0.39	0.306	0.202

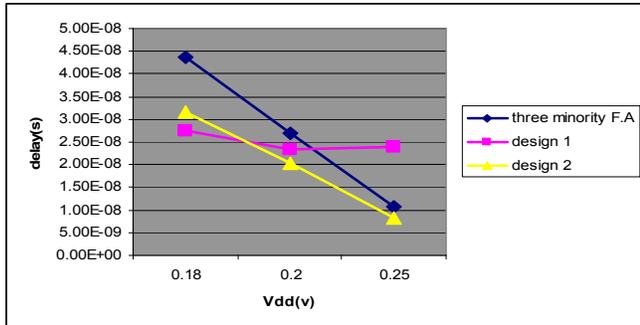
7. SUMMARY AND CONCLUSION

Two novel low-power 1-bit full adder cells have been proposed. The first design uses majority-not, NAND and NOR gates which are implemented using 6 transistor in subthreshold region. The second design uses two majority-not gates, which the first majority-not gate has three inputs and the second majority-not gate has five inputs in subthreshold region. The second design and the first design have fewer transistors than minority-3 based 1-bit full adder. Low power consumption has been targeted at the circuit design level for both cells. Simulations were done at three supply voltages, ranging from 0.25v down to 0.18v by 65nm, 90nm and 0.18um technologies. Results have shown that our circuits had the least power consumption and PDP in most cases in comparison with minority-3 based 1-bit full adder.

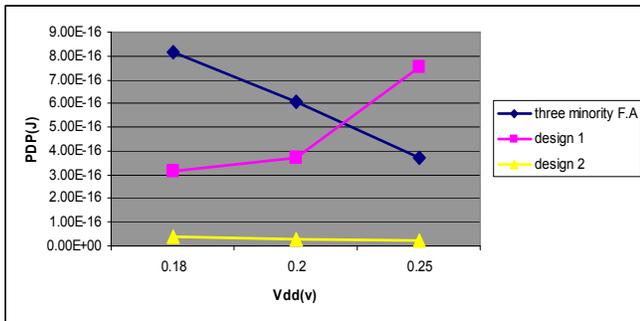




(a)



(b)

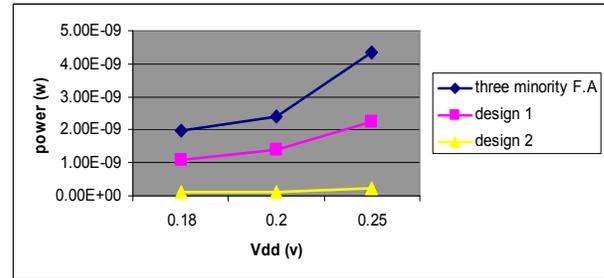


(c)

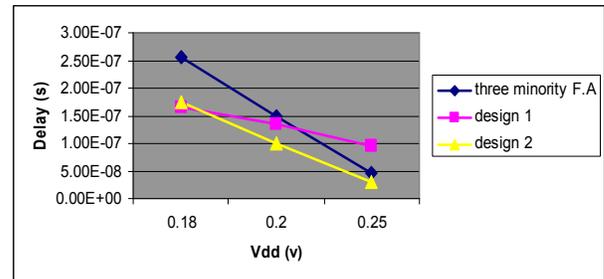
Figure 7. (a) Power versus supply voltage in 65nm technology (b) Delay (c) PDP

Table 3: values for power, delay and PDP in 90nm technology

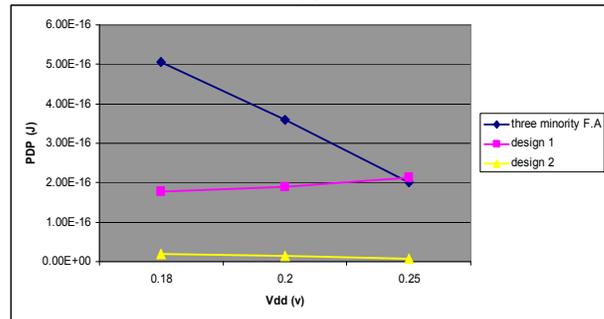
Supply voltage(v)	0.18	0.2	0.25
Power(*e-10 w)			
Minority-3 based 1-bit F.A (26T)	1.98	2.42	4.33
Design1 (22T)	1.08	1.39	2.24
Design2 (22T)	0.107	0.131	0.22
Delay(*e-7 s)			
Minority-3 based 1-bit F.A (26T)	2.56	1.48	0.463
Design1 (22T)	1.64	1.36	0.947
Design2 (22T)	1.74	1.01	0.312
PDP(*e-17 J)			
Minority-3 based 1-bit F.A (26T)	50.6	35.8	20
Design1 (22T)	17.7	18.9	21.2
Design2 (22T)	1.86	1.32	0.68



(a)



(b)

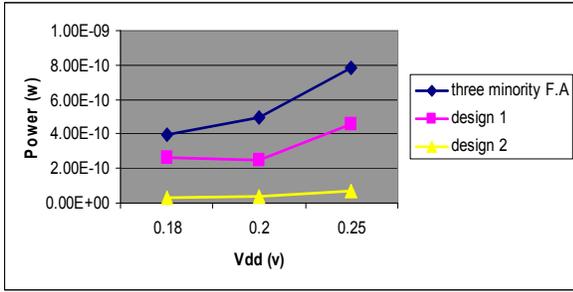


(c)

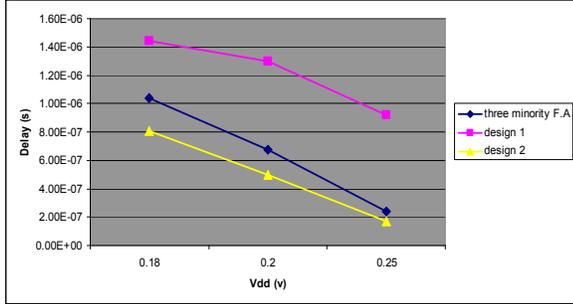
Figure 8. (a) Power versus supply voltage in 90nm technology (b) Delay (c) PDP

Table 4: values for power, delay and PDP in 0.18um technology

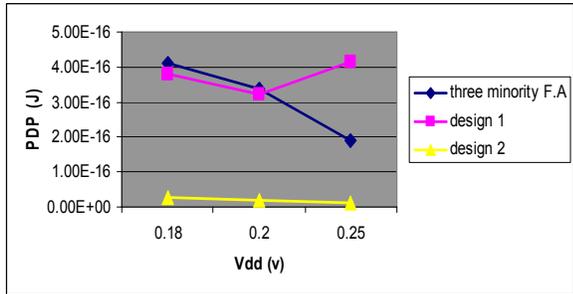
Supply voltage(v)	0.18	0.2	0.25
Power(*e-10 w)			
Minority-3 based 1-bit F.A (26T)	3.96	4.98	7.81
Design1 (22T)	2.64	2.49	2.54
Design2 (22T)	0.324	0.401	0.696
Delay(*e-7 s)			
Minority-3 based 1-bit F.A (26T)	10.4	6.75	2.42
Design1 (22T)	14.4	13	9.17
Design2 (22T)	8.09	4.96	1.71
PDP(*e-17 J)			
Minority-3 based 1-bit F.A (26T)	41.1	33.6	18.9
Design1 (22T)	38	32.3	41.6
Design2 (22T)	2.62	1.99	1.19



(a)

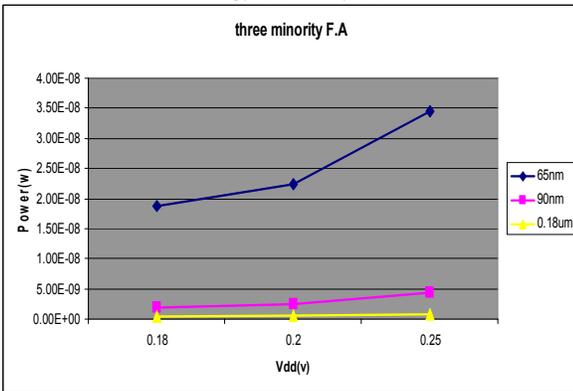


(b)

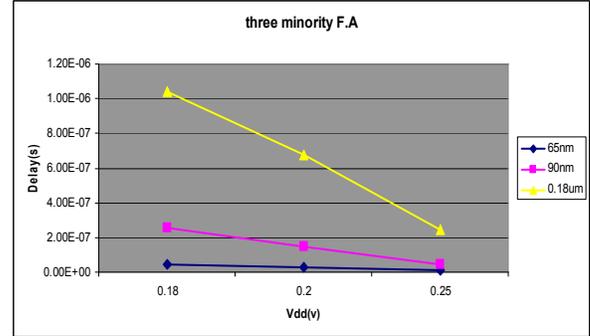


(c)

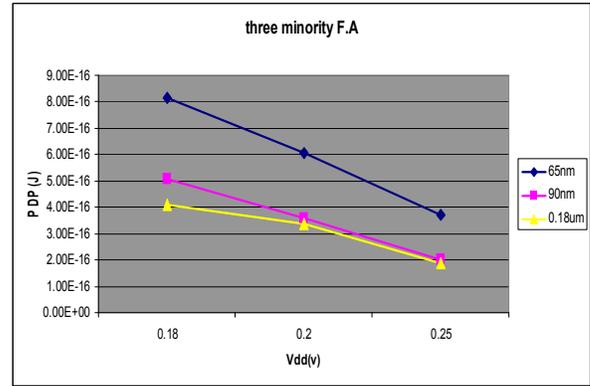
Figure 9. (a) Power versus supply voltage in 0.18um technology (b) Delay (c) PDP



(a)

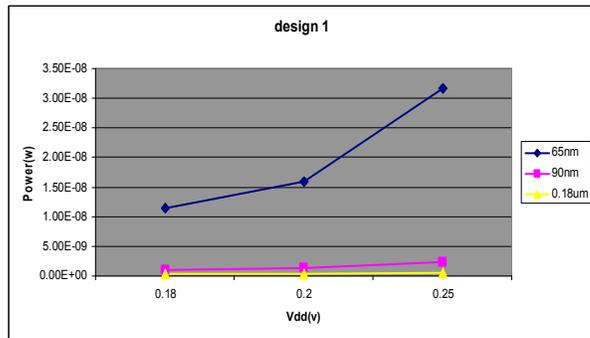


(b)

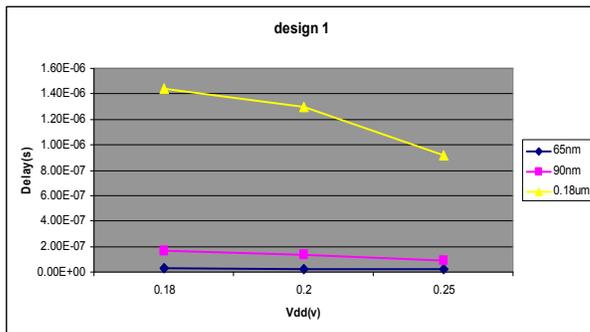


(c)

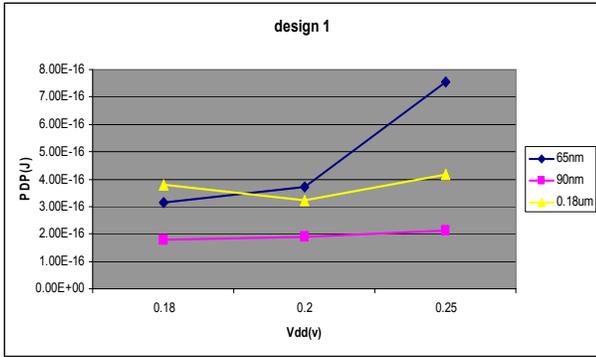
Figure10. (a) Power versus supply voltage in all of three technologies for minority-3 based 1-bit full adder (b) Delay (c) PDP



(a)

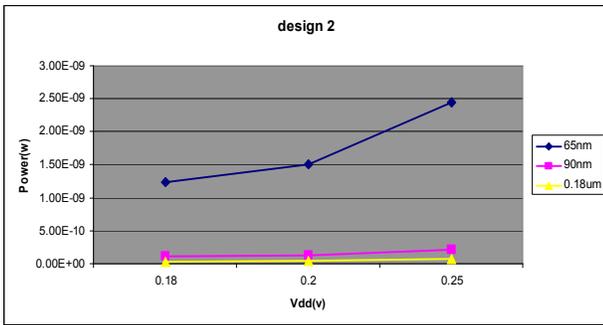


(b)

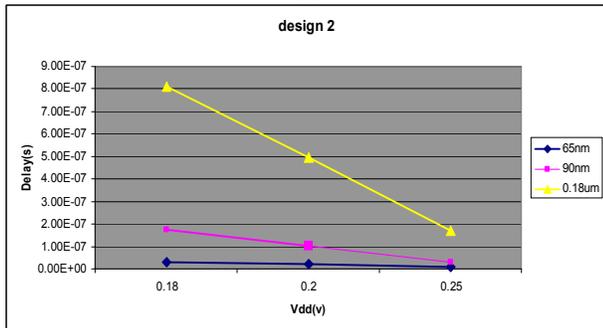


(c)

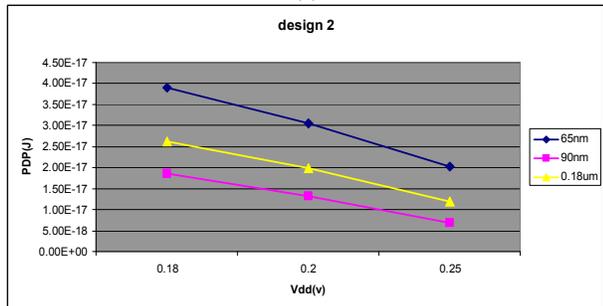
Figure11. (a) Power versus supply voltage in all of three technologies for design 1(b) Delay (c) PDP



(a)



(b)



(c)

Figure12. (a) Power versus supply voltage in all of three technologies for design 2 (b) Delay (c) PDP

8. REFERENCES

- [1] Aunet, S., Oelmann, B., Abdalla, S. and Berg, Y. 2004. "Reconfigurable Sub-threshold CMOS Perceptron," International Joint Conference on Neural Networks, IJCNN, pp. 1983-1988.
- [2] Aunet, S. 2007. Kretselement U.S. Patent 7,288,968.
- [3] Granhaug, K. and Aunet, S. 2006. "Six Subthreshold Full Adder Cells characterized in 90 nm CMOS technology," DDECS, pp. 27-32.
- [4] Aunet, S. and Beiu, V. 2005. "Ultra low power fault tolerant neural inspired CMOS logic," in Proc. IEEE Int. Joint Conf. Neural Network, pp. 2843-2848.
- [5] Aunet, S. 2003. Kretselement, Norwegian patent application, no. 20035537, Leiv Eiriksson Nyskapning, Trondheim, Norway.
- [6] Moalemi, V. and Afzali-Kusha, A. 2007. "Sub Threshold 1 Bit Full Adder Cells in Sub100 nm Technology," IEEE Computer Society Annual Symposium on VLSI, pp. 514-515.
- [7] Soeleman, H., Roy, K. and Paul, B.C. 2001. "Robust subthreshold logic for ultra-low power operation," IEEE Trans. VLSI Syst.
- [8] Aunet, S., Oelmann, B., Andreas, P. and Berg, Y. 2008. "Real-Time Reconfigurable Subthreshold CMOS Perceptron," IEEE Transaction On Neural Network, Vol.19, No.4, pp. 645-657, APRIL 2008.
- [9] Razavi, B. Design of Analog CMOS Integrated Circuits.
- [10] Navi, K., Moaiyeri, M.H., Faghih Mirzaee, R., Hashemipour, O. and Mazloom Nezhad, B. 2009. "Two novel low-power full adders based on majority-not gates", Elsevier, Microelectronics Journal, Vol. 40, Issue. 1, pp. 126-130.
- [11] Shams, A.M. and Bayoumi, M.A. 2000. "A Novel High-Performance CMOS 1-bit Full Adder Cell," IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing, Vol. 47, No. 5, pp. 478-481, May 2000.
- [12] Shams, A.M., Darwish, T.K. and Bayoumi, M.A. 2002. "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 1, pp. 20-29, Feb. 2002.