First Order Sigma Delta Modulator Design using Floating Gate Folded Cascode Operational Amplifier

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ABSTRACT
Power consumption is the major issue in VLSI design. In this paper an efficient low power first order sigma delta modulator is designed for oversampled ADC using floating gate folded cascode operational amplifier, in 0.35 µm Technology. Floating gate MOSFET have low power Dissipation hence it is an attractive solution in design of data converters, low voltage op-amp with rail-to-rail input and the four quadrant multiplier circuits in low-voltage analog signal processing. This paper firstly concerns with determination of nonidealities. The nonidealities investigated are clock jitter, thermal noise, circuit leakage, and limited slew rate and gain bandwidth product of Opamp. These all nonidealities are overcome here by using folded cascode Opamp at integrator stage with DC gain 56db ,slew rate of 3.633v/µs ,and gain bandwidth product 14.6MHz .Finally, a first order sigma delta modulator implemented using power supply of ±2.5V using Tanner EDA.

General Terms
VLSI Circuit Design, Experimentation, Performance, Simulation.

Keywords
Modulator, Floating Gate, Nonidealities.

1. INTRODUCTION
Now a days mixed signal circuits are filling the gap between analog and digital circuits which reduces the size of system, increases speed of operation, reduces power dissipation and increases design flexibility. Data converters are the core components of the mixed signal systems

Sigma delta modulator is one of the attractive mixed signal system, which has gained importance because of the development in digital VLSI technologies which provide practical means to implement large Digital signal processing circuitry .A requirement of analog to digital converter is compatibility with VLSI technology, in order to provide for monolithic integration of both the analog and digital sections on single die.

In sigma delta modulation, sigma suggests a summing operation and delta modulation indicates the process which utilizes quantization of the change in the signal from sample to sample rater than the absolute value of the signal at each sample.

Figure 1 shows the block diagram of proposed First order sigma delta modulator. It consist of integrator, a comparator, D-latch and Digital to analog converter (D/A) [3].

In this paper Integrator is designed using folded cascode Opamp with consideration of nonidealities. The non idealities investigated are clock jitter, thermal noise, circuit leakage, and limited slew rate and gain bandwidth product of Opamp. These all nonidealities are overcome here by using folded cascode Opamp at integrator stage with DC gain 56db, slew rate of 3.633v/µs, and gain bandwidth product 14.6MHz .Finally, a first order sigma delta modulator implemented using power supply of ±2.5V.

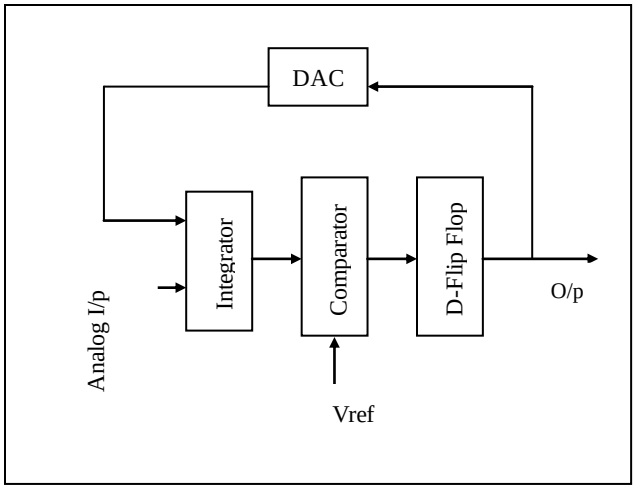

Figure 1 Block Diagram Of One Bit Sigma Delta Modulator

2. INTEGRATOR DESIGN
Integrator is the most important component in sigma delta modulator. In this paper, Switched capacitor (SC) integrator is designed, therefore no need to use sample and hold circuit. This non inverting SC integrator consist of folded cascode Opamp, a sampling capacitor, an integrating capacitor (CI) and four MOS switches as shown in Figure 2. Two non-overlapping clock controls are required as input to the MOS switches. In sigma delta ADC, output of DAC controls one clock whereas Analog

input acts as another control clock. Common mode input is chosen 0v.

Integrator operates as follows

$$vout = \frac{Cs}{C_I}\frac{z^{-1}}{1-z^{-1}}$$

In order to make the first order modulator loop stable, gain of the integrator is chosen less than 1 i.e. 0.5 with Cs=1pf and CI=2pf. Even smaller capacitances can be used but to avoid charge leakage problem they are taken high [1].

Simulation of Opamp gives 0.598mv input offset voltage, 56db DC gain, 14.6MHz bandwidth, 53.19 phase margin, and 3.633v/µs slew rate as shown in figure 4, 5 & 6.

3. COMPARATER DESIGN

One bit comparator designed here consists of M1 and M2 transistors as input driver. If integrator output is greater than the reference voltage then the comparator gives an output '1' and if integrator output is less than the reference voltage, then the output of the comparator is '0'. The implemented comparator is as shown in figure 7.

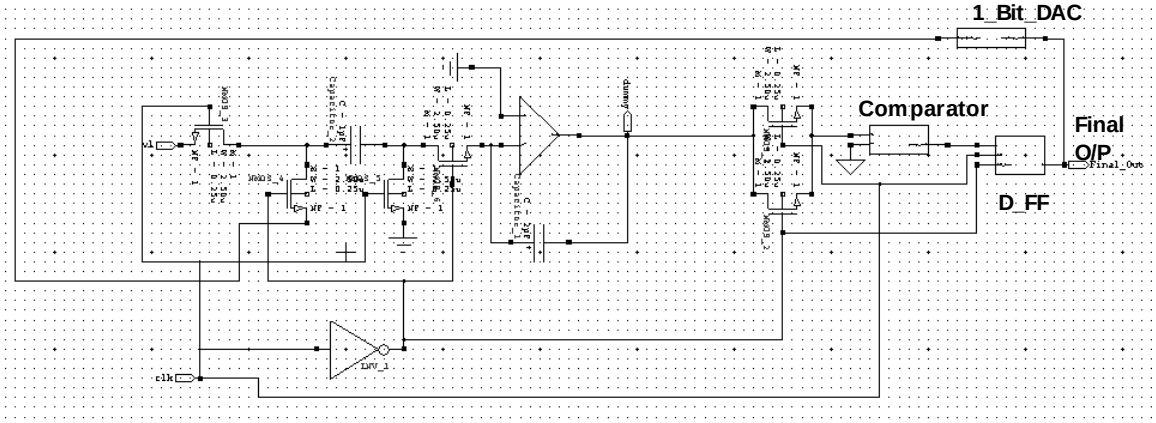

Figure 2 One Bit Sigma delta modulator

2.1 FOLDED CASCODE OPAMP DESIGN

In this paper integrator is designed using floating gate folded cascode Opamp. Where MOSFET's has floating gate at input stages .folded cascode Opamp is a good choice for design as it is a wide band, fast settling amplifier. Two stage Opamp suffers from frequency degradation of power supply rejection ratio, which can be overcome by using it. It also provides high gain, easier frequency compensation. In addition to this floating Gate MOS is used here, which can be use to hold charge on the gate to shift its threshold voltage.

In this design differential pair is formed by P-channel MOSFET's M1, M2. The first stage gives a high differential gain and performs the differential to single ended conversion. This first stage of Opamp also had the current mirror circuit formed by an n-channel MOSFET M3 and M4. Transistor M6 serves as an n channel common source amplifier which is the second stage of Opamp and is aided by current load M5. The bias of the Opamp circuit is provided by M8 and M9 transistors. This is shown in figure 3.

4. ONE BIT DAC

In one bit DAC reference voltages are +Vref and -Vref are +2.5V and -2.5V respectively. If digital input is 1 then output of DAC is Vref and If digital input is '0' then output of DAC is –Vref. The implemented one bit DAC is as shown in figure 8.

5. NONIDEALITIES

5.1 Clock jitter at the comparator

Timing jitter in the quantizer clock is usually called clock jitter. This sampling clock jitter results in non uniform sampling and increases the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal to the converter [2]. This can be overcome by proper selection of oversampling ratio.

5.2 Thermal Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidth of Op-Amps. Therefore, it must be taken into account for both the switches and the Op-Amps in switched capacitor circuits [3].

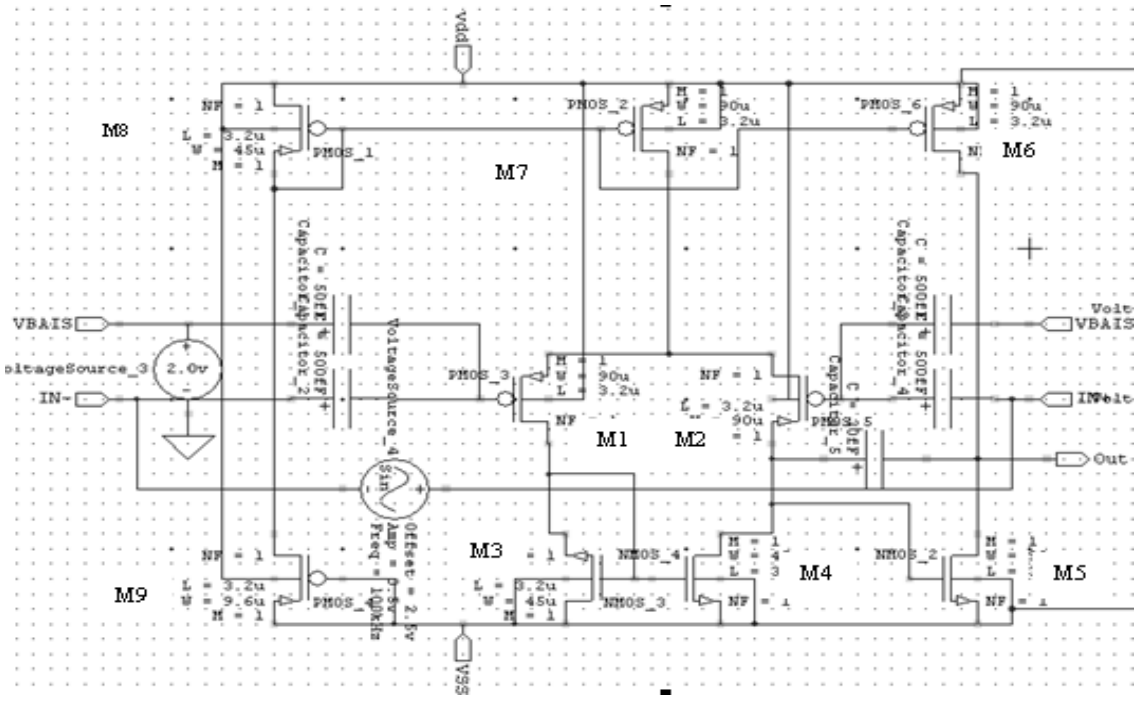

Figure 3 Floating gate Folded Cascode Opamp

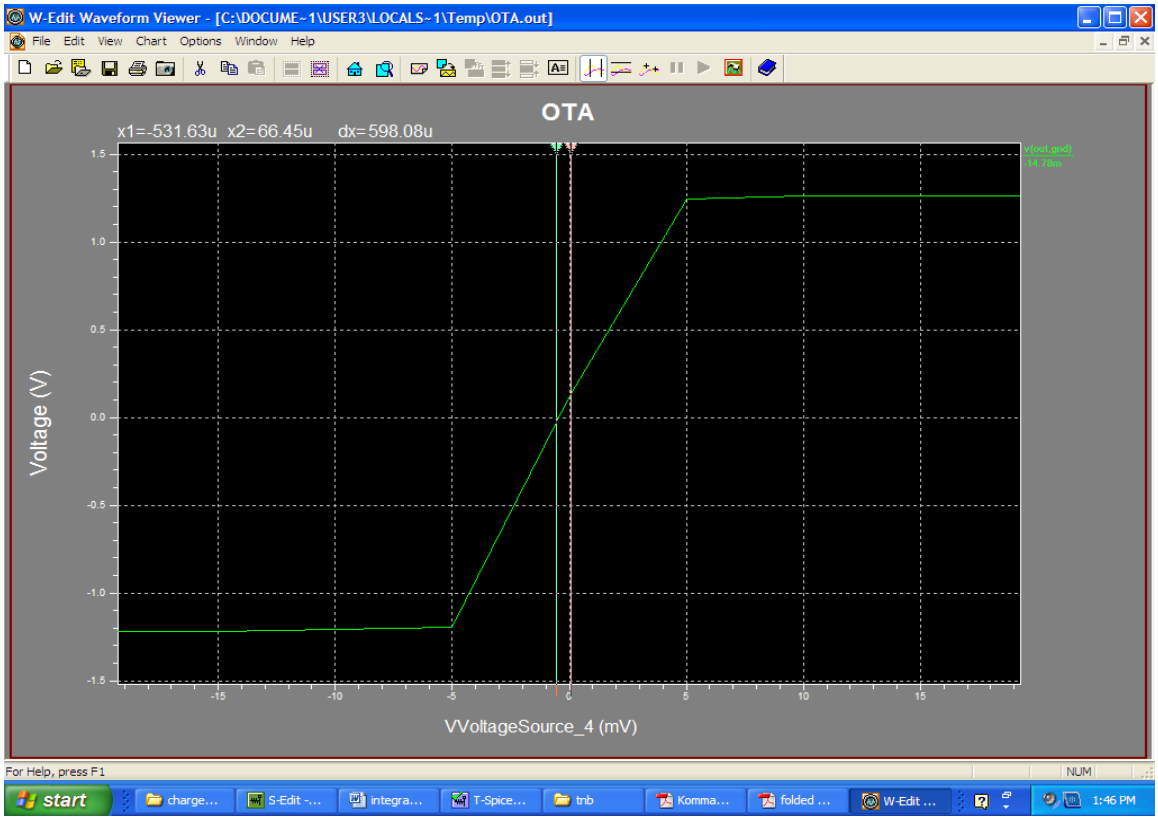

Figure 4 Transfer Characteristics of Opamp

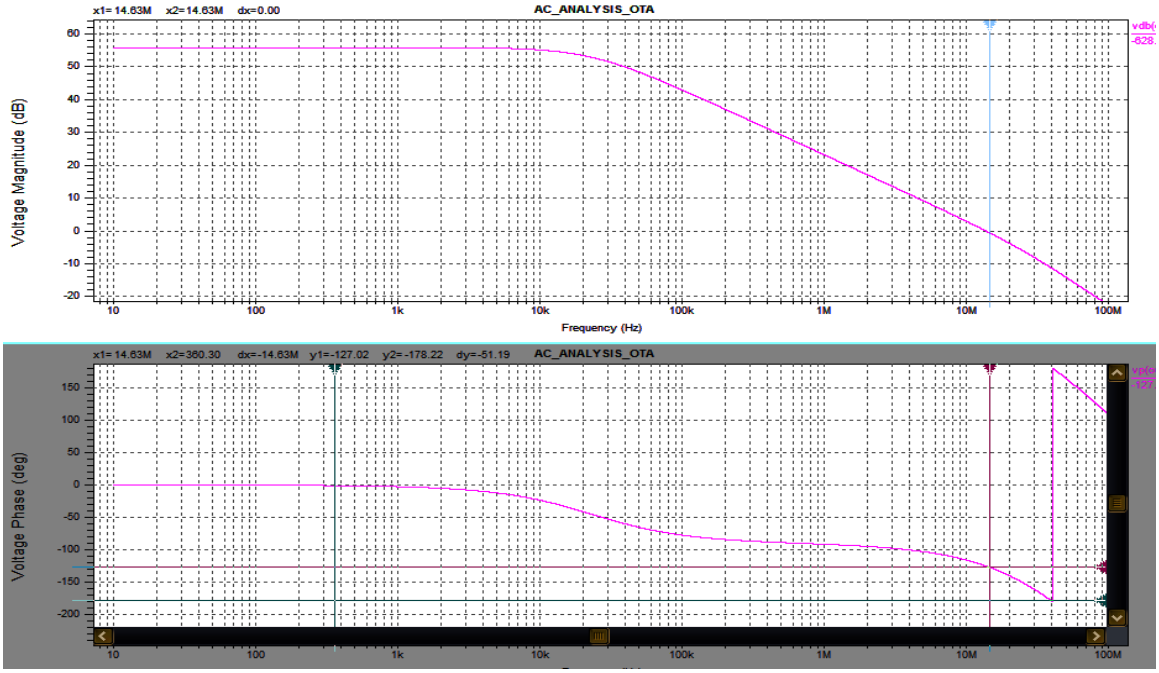

Figure 5: AC Analysis of Opamp

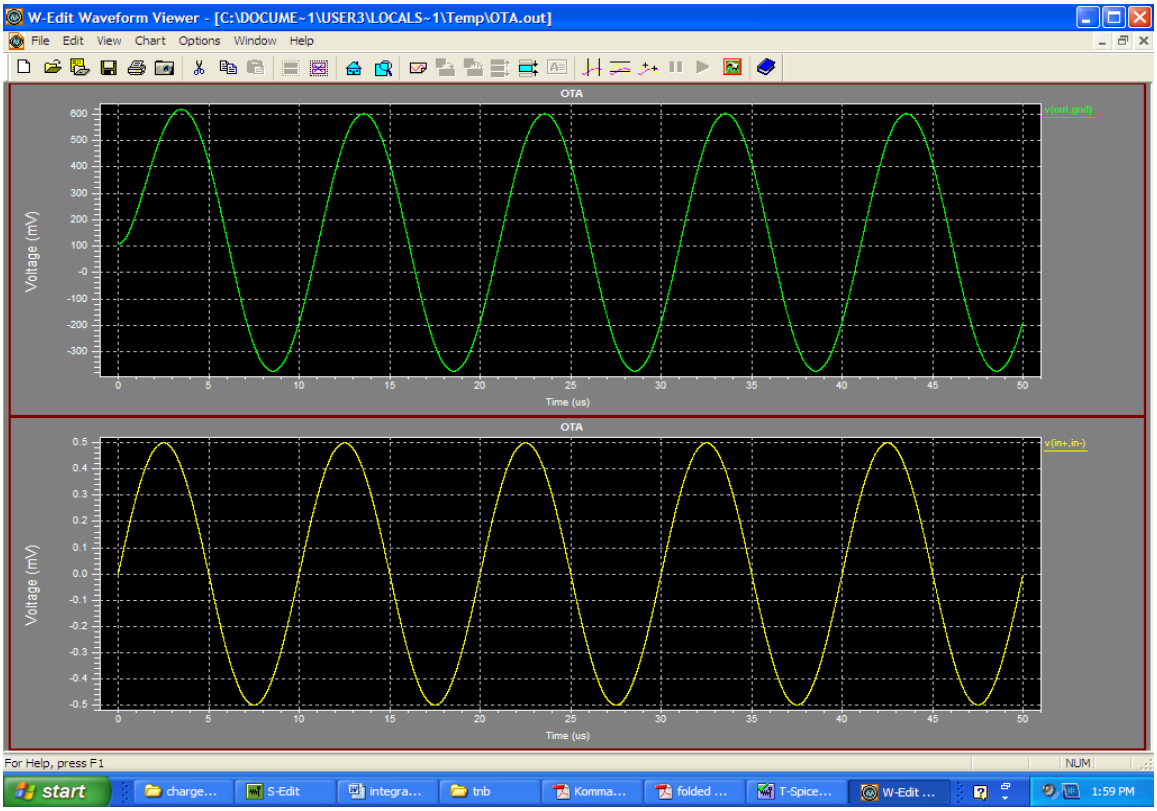

Figure 6 Transient Analysis of Opamp

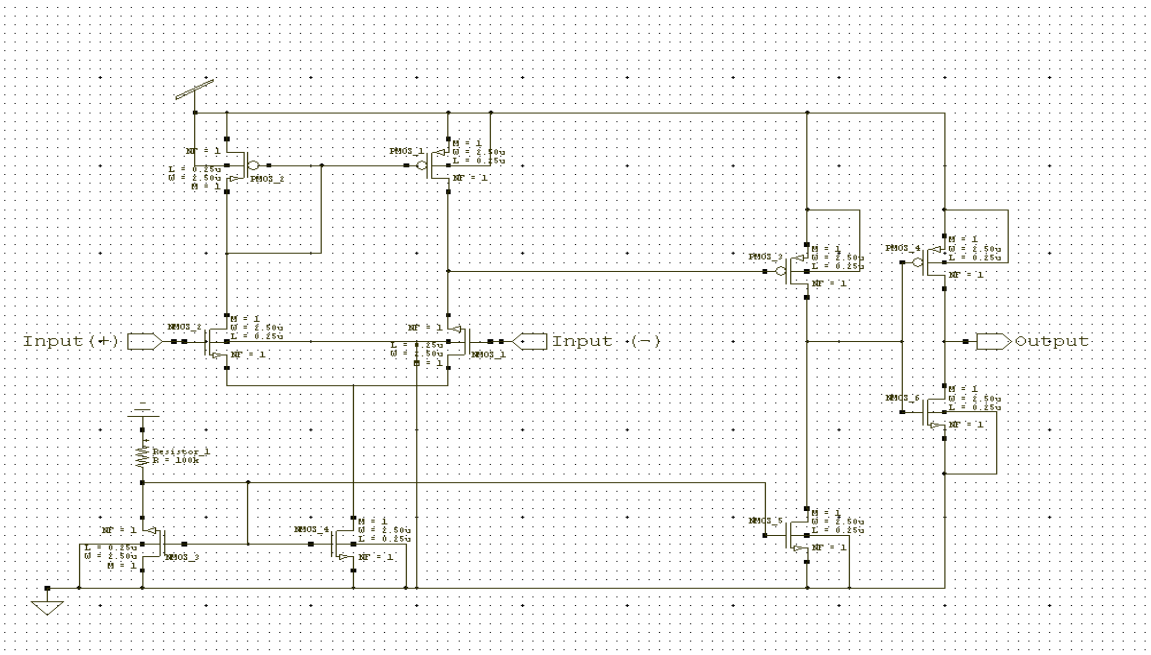

Figure 7 One bit Comparator

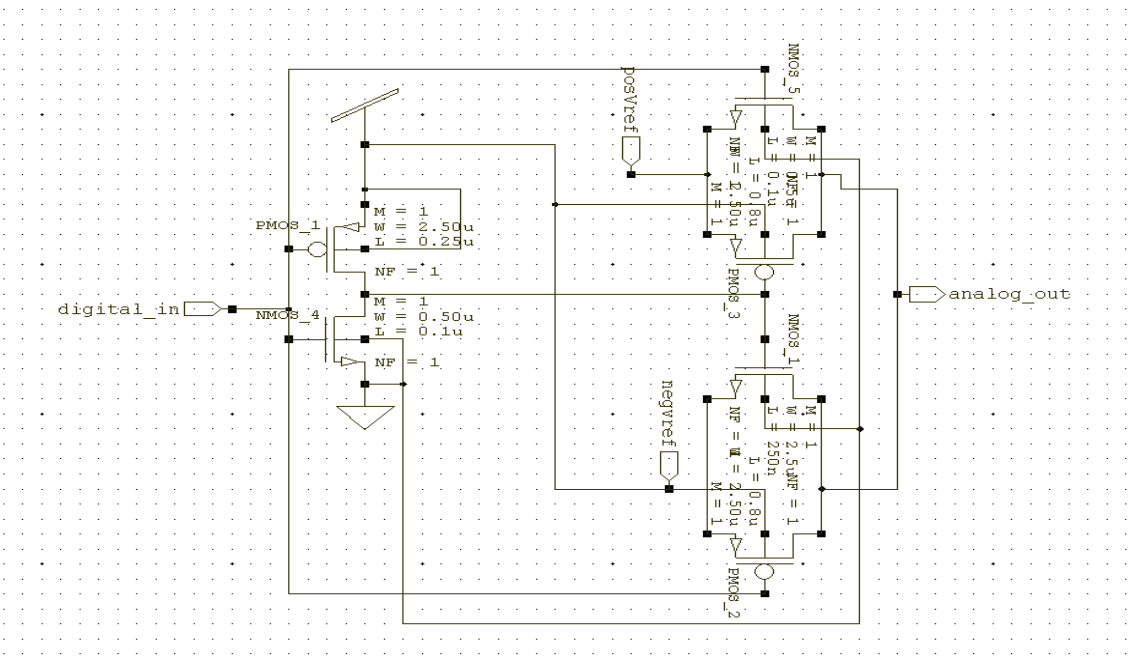

Figure 8 One bit DAC

5.3 Integrator Nonidealities

Most of the nonidealities of Sigma delta modulator are located in the integrator. The nonidealities considered are leakage due to finite gain, finite Bandwidth, Slew rate, saturation and nonlinearity of the amplifier.

6. SIMULATION RESULT

Figure 9 shows, output is '1' if input +Vref > 0, otherwise it is '0'. In Sigma delta modulator, if integrator output is greater than the reference voltage then the comparator has to give an output of '1' and if integrator output is less than the reference voltage, then the output of the comparator should be '0'.

Figure 10 Shows output waveform for one bit DAC where for digital input output varies between +2.5v to -2.5v.

Figure 11 shows that practical results are not matching exactly with theoretical results, but characteristics of modulator are still following the track. Main cause of this variation is integrator which adds quantization noise.

DC gain of the ideal integrator is infinite, but due to circuit constraints it is not infinite for real system [6] [7] [8]. This causes leaky integration of the output from the input of the integrator.

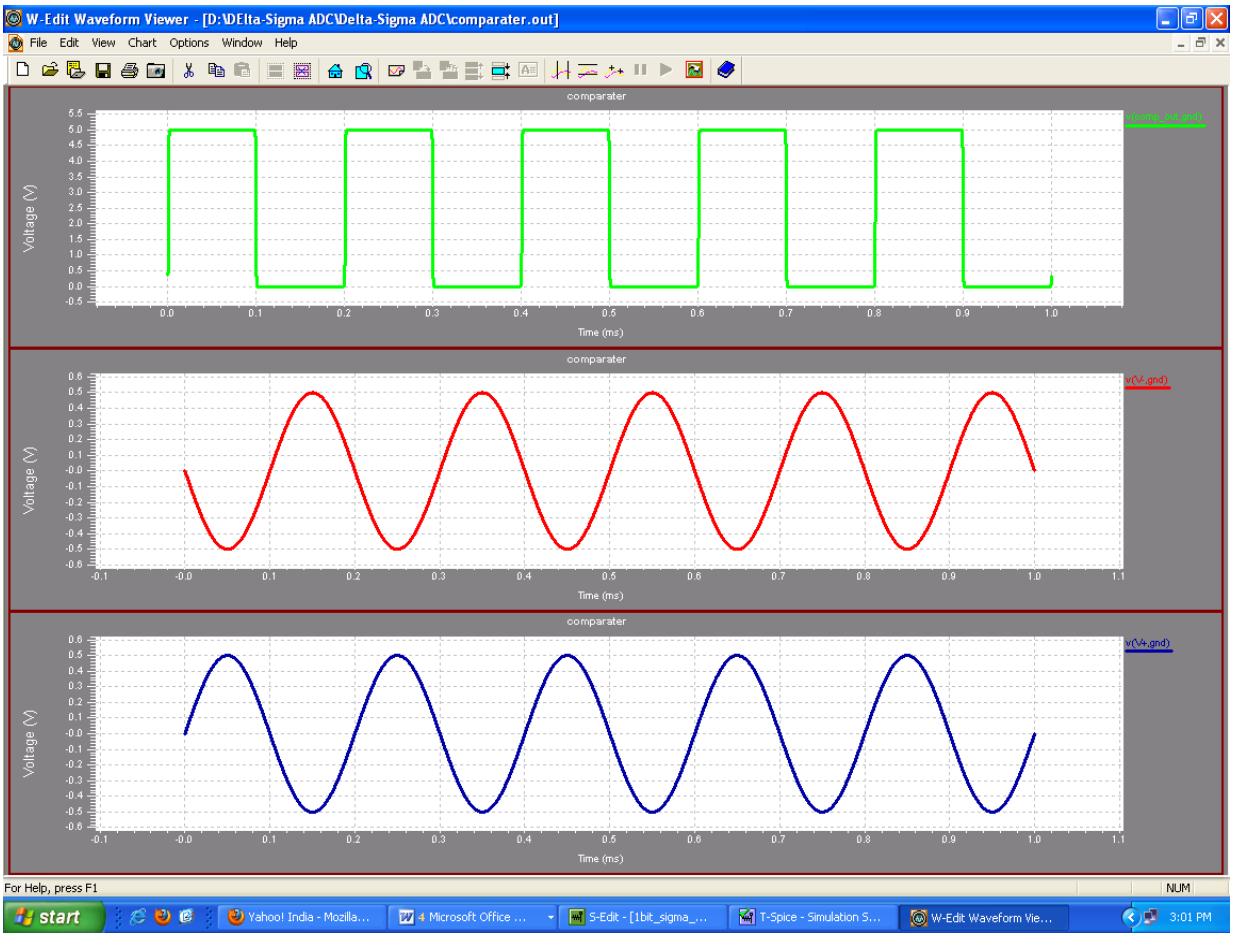

Figure 9 Results of One bit Comparator

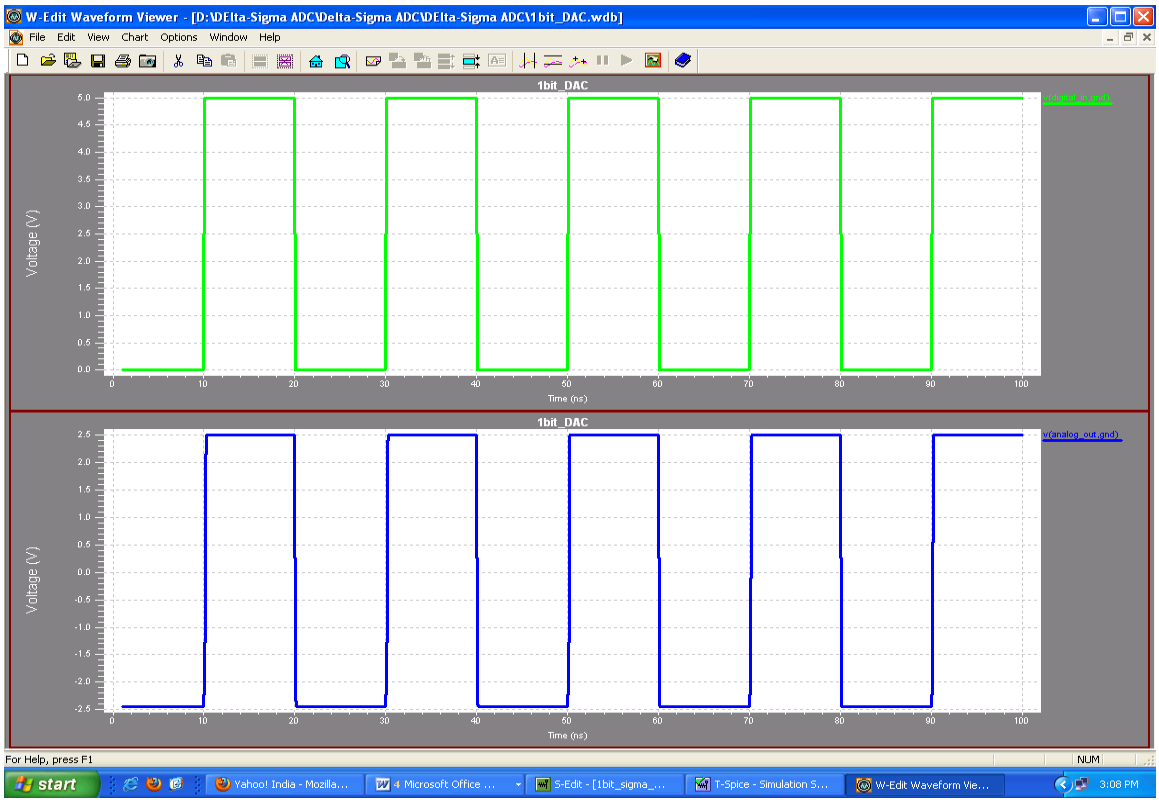

Figure 10 output waveforms of One bit DAC

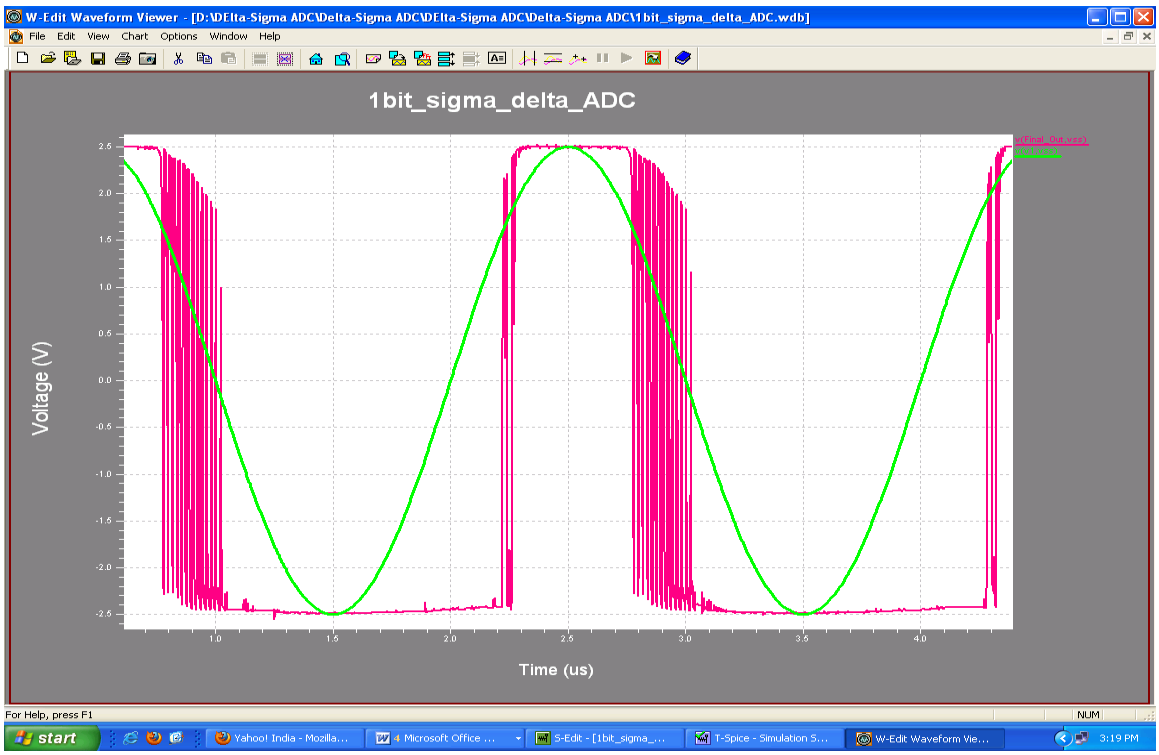

Figure 11 Output waveforms of One Bit Sigma delta modulator

7. CONCLUSION

First order sigma delta designed here using switched capacitor integrator still undergoes under nonidealities even though it is investigated. Output characteristics are not matching exactly with theoretical results but keeping the trend of modulator .Non idealities are overcome here up to some percent using folded cascode Opamp at integrator stage with DC gain 56db, slew rate of 3.633v/μs, and gain bandwidth product 14.6 MHz. Finally, a first order sigma delta modulator implemented using power supply of ± 2.5V in 0.35 μm technology using Tanner EDA.

8. REFERENCES

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