Hetero double gate-dielectric Tunnel FET with record high I_{ON} /I_{OFF} ratio

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ABSTRACT
To manage the increasing static leakage in low power applications and reduced I_{on}/I_{off} due to aggressive scaling of MOS transistors, Tunnel FET (TFET) devices are considered as the most promising candidates because of their excellent immunity against such important short channel effects. Solutions for leakage reduction as well as improving on current of the device are sought at the device design and process technology levels. In this paper, we propose a novel design for a hetero double gate dielectric tunnel field effect transistor (HDG-TFET). Simulation of this device characteristics show significant improvement over conventional double gate devices with high K only gate dielectric TFET. In this device, a low K gate oxide is used at the drain end and a high K gate oxide is used at the source end with low band gap material in source region. Ambipolar behavior at the drain end can be suppressed and a record high I_{on}/I_{off} of the order of 10^{13} is achieved.

General Terms
Device simulation .

Keywords
Ambipolar transport, heterogate-dielectric, band-to-band tunneling.

1. INTRODUCTION
To achieve high speed and packing density in VLSI, continuous scaling of MOSFET gives rise to short channel effects. Tunnel field transistor is considered as one of the most promising alternatives to provide scaling benefits with significant suppression of the SCEs. High on current can be maintained and low off current in case of HDG-TFET. This approach is motivated by the fact that the conduction mechanism in tunnel FET is completely different from MOSFET, which is based on band-to-band tunneling [1, 2]. The small band-to-band tunneling efficiency in large bandgap silicon results not only low off current but also low on current and severe ambipolar behavior material. which leads to parasitic conduction in off state. Solutions to low on current, low on/off ratio and ambipolar behavior issues exist based on material and device structure optimization.To improve $I_{on,}$ high K material has been introduced as a gate dielectric [2]. High K material used as gate insulator may increase undesirable leakage current (ambipolar) [4].

In this paper, we propose a HDG-TFET for higher on current and lower ambipolar current. Lower band gap material is used in the source side for enhancing the band-to-band tunneling generation rate which is an exponential function of the bandgap. The use of Germanium in the source region where band-to-band tunneling occurs leads to high on/off current ratio . The HDG-TFET uses different gate dielectric materials at the drain and source side, which can be formed by isotropic etching of silicon dioxide followed by high K material deposition [2, 6]. The proposed HDG-TFET is compared with high K only Double gate TFET. The gate length is equal to L_{sio2} and $L_{high\ k}$ lengths. But DG-TFET where only high K is use, L_G is equal to the $L_{high\,k}$.

2. DEVICE- DESIGN AND OPERATION
The proposed device is a lateral type hetero double gate dielectric TFET which is a gated p-i-n diode as shown in Figure 1. Tunneling takes place in this device between the intrinsic and p^+ regions. To operate the device, the source is grounded and 1 volt is applied to the drain, and 1.5 volt is applied to the gates. As the gate voltage is increased the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow [4, 5]. In order to determine the merits of proposed HDG-TFET structure, the results have been compared with high K DG-TFET Fig. 2. using 2D device simulation, Synopsis TCAD tools. A non-local band-to-band tunneling model [5] has been used. In this simulation, L_G used is 30 nm, thickness of silicon is 25 nm, oxide thickness is 3 nm, and the gate insulator high K material is HfO_2. The doping concentration of drain, channel, and source are 5×10^{19}, 1×10^{17}, $1\times10^{22}cm^{-3}$.

3. RESULTS AND DISCUSSIONS
In case of double gate Tunnel FET, the on current will be at least double due to the presence of an added gate compared to single gate tunnel FET [2]. In HDG-TFET, a part of the insulator is given is high K material located near the source side. Electrons tunnel from the valence band in p^+ source to the conduction band in intrinsic body then move toward the n^+ drain by drift

diffusion. Tunneling occurs in the region of high electric field, where local band bending is more than the band gap. This bending is due to gate voltage which decreases the length of tunneling path abruptly. For various lengths of L_{highK}, I_D - V_{GS} characteristics shown in Figure 3 are observed. When L_{highK} is increased the conduction band well becomes wider, leading to less abrupt transition between on and off states. When L_{highK} is about 5 nm for L_G= 30nm, best result is obtained.

Next, we present the HDG-TFET that utilizes Germanium as source region to achieve a small bandgap, and hence, high I_{on}/I_{off} ratio of 10^{13} [6, 7]. We derive a basic analytical formulation of tunneling probability considering triangular potential barrier and applying WKB approximation. Tunneling probability by

$$T(E) = \exp\left(-\frac{4\pi\lambda\,(2m^*)^{1/2}\,E_g^{3/2}}{q\,(E_g+\Phi_F)\,h}\right)$$

where λ is the tunnel junction width, m^* is the effective mass of electron, Eg is the forbidden gap, h be the Planck constant, and Φ_F is the energy range over which tunneling takes place. Therefore use of low bandgap material, like germanium, increases the tunneling probability. In the proposed HDG-TFET, the ambipolar current (I_{amb}) is defined as drain current when V_G=-0.2 V, V_D=1V. I_{amb} is reduced due to the presence of SiO_2 gate dielectric at the drain side because drain side gate insulator has lower dielectric constant than the same on the source side. Device gate length has been optimized in order to get a maximum on current [8]. At lower value of gate lengths,

i.e. 20 nm, the on /off current ratio is less because tunneling takes place in off state also due to reduced channel length. On the contrary, at higher gate lengths i.e at 50 nm I_{on} /I_{off} ratio are also less due to reduced abrupt transition between on and off states. The optimized gate length is 30nm Figure 4.

4. CONCLUSION

The investigated HDG-TFET shows improved characteristics over high K DG-TFET after proposing device modifications: hetero gate dielectric, low bandgap material and optimized device structure. High K material on the source side induces a local minimum of the conduction band edge E_c at the tunneling junction. A record high on/off ratio of 10^{13} is obtained for L_{highk}=5nm, L_G=30nm and germaniumsource HDG-TFET which have been proposed for high performance and low power consumption.

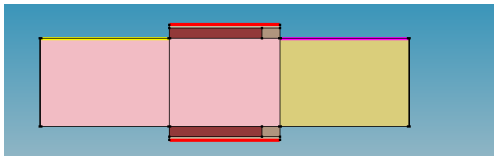

Fig 1. H DG-TFET

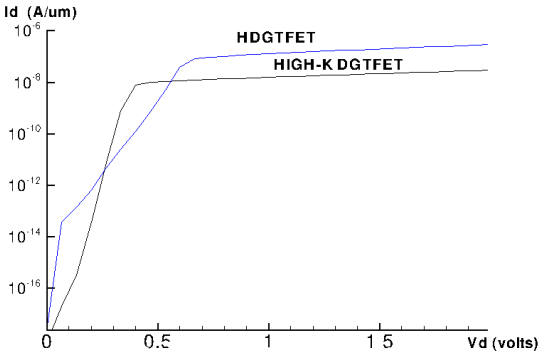

Fig 2. I_d-V_d curves for H DG-TFET and HIGH K DGTFET

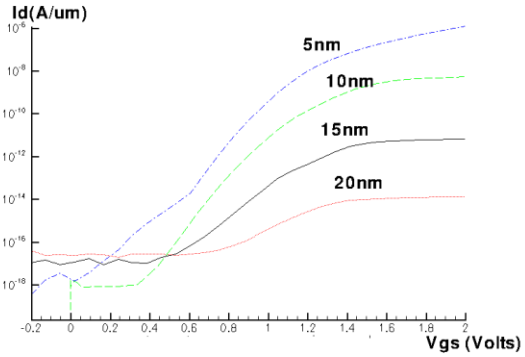

Figure 3. Id -Vgs characteristics for different L_{highK} for L_G = 30nm

Table 1. I_{on}/I_{off} ratio for various L_{highk}, L_G=30nm

L_{highk}	5nm	10nm	15nm	20nm
I_{on}/I_{off}	10^{13}	10^{9}	10^{6}	10^{2}

Table 2. I_{on}/I_{off} ratio for various L_G for L_{highK}=10nm (Figure 5)

L_G	20nm	30nm	40nm	50nm
I_{on}/I_{off}	10^4	10^9	10^9	10^2

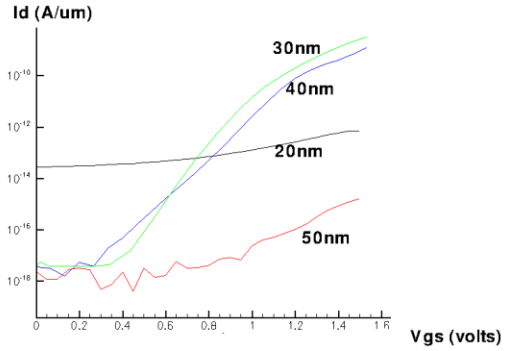

Figure 4. Id – Vgs curves for various

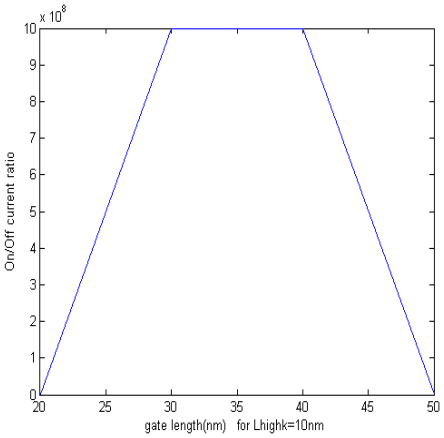

Figure 5. On/Off current ratio for various L_G , L_{highK} = 10nm gate lengths, L_{highK}=10nm

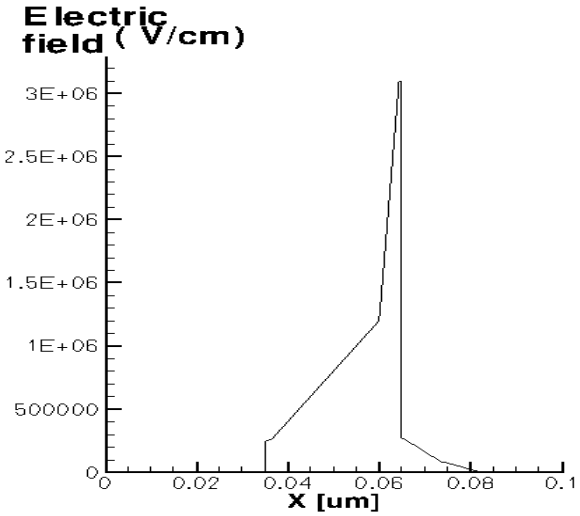

Figure 6. Lateral electric field along channel

5. ACKNOWLEDGMENTS

Our thanks to the experts who have contributed towards the development of the template.

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