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On the Design of High-Performance CMOS 1-Bit Full Adder Circuits

Shivshankar Mishra
Programme 'AD'
Defence Research and Development Organization
Hyderabad-500058, India

V. Narendar
Department of Electronics and Communication Engineering
Motilal Nehru National Institute of Technology
Allahabad-211004, India

Dr. R. A. Mishra
Department of Electronics and Communication Engineering
Motilal Nehru National Institute of Technology
Allahabad-211004, India

ABSTRACT
In this paper, two high performance full adder circuits are proposed. We simulated these two full adder circuits using Cadence VIRTUOSO environment in 0.18 μm UMC CMOS technology and compared the Power dissipation, time delay, and power delay product (PDP) of the proposed circuits with other 10 transistor full adders. Simulation results show that for the supply voltage of 1.8V, these circuits are suitable for arithmetic circuits and other VLSI applications with very low power consumption and very high speed performance.

Keywords
CMOS logic, Full adder, High-performance, Threshold loss

1. INTRODUCTION
Adder is one of the most important components of a CPU (central processing unit), Arithmetic logic unit (ALU), floating-point unit and address generation like cache or memory access unit use it. In addition, Full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. Arithmetic functions such as 'addition', 'subtraction', 'multiplication' and 'division' are some examples, which use 'adder' as a main building block. As a result, design of a high-performance full-adder is very useful and important [1]-[3].

On the other hand, increasing demand for portable equipments such as cellular phones, personal digital assistant (PDA), and notebook personal computer, arise the need of using area and power efficient VLSI circuits. Low-power and high-speed adder cells are used in battery-operation based devices.

In this paper, we present two different 1-bit full-adder circuits, with suitable power consumption, delay performance. We have simulated these two Full-adders circuit along with various 10 transistors full adder circuits and compared the Power dissipation, propagation delay, and power delay product (PDP) of the proposed cells with other 10 transistor full adders.

The basic advantage of 10 transistors full adders [4]-[7] are-low area compared to higher gate count full adders, lower power consumption, and lower operating voltage. It becomes more and more difficult and even obsolete to keep full voltage swing operation as the designs with fewer transistor count and lower power consumption are pursued. In pass transistor logic [8]-[9], the output voltage swing may be de-graded due to the threshold loss problem. That is, the output high (or low) voltage is deviated from the V_{DD} (or ground) by a multiple of threshold voltage V_T. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. At low V_{DD} operation, the degraded output may even cause malfunction of circuit. Therefore, for designs using reduced voltage swing, special attention must be paid to balance the power consumption and the speed.

SERF (static energy recovery full adder) [10]-[12] is shown in Fig.1 (a). This uses a total of 10 transistors for the implementation of following logic expressions.

$$Sum = (A\overline{\oplus}B)C_{in} + (A \oplus B)\overline{C_{in}} \quad (1)$$

$$C_{out} = (A \oplus B)C_{in} + (A\overline{\oplus}B)A \quad (2)$$

The design is claimed to be extremely low power because it doesn't contain direct path to the ground and it can re-apply the load charge to the control gate (energy recovery). The combination of low power and low transistor count makes the SERF adder cell a feasible option for low power design. But the disadvantage with this design is relatively slower than peer designs and it cannot be cascaded at low V_{DD} operation due to multiple-threshold loss problem.

The 9A Full adder shown in Fig. 1(b) implements (1) and (2) using 4-transistor SER XNOR, 4-transistor ground less XNOR and 2-to-1 multiplexer [10]-[12].

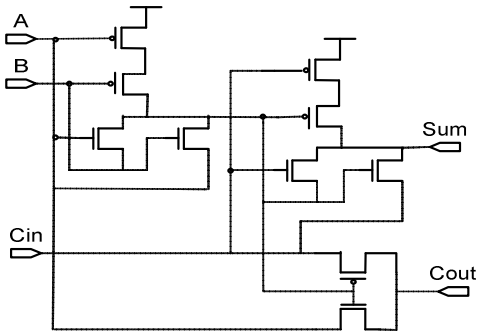
The 9B Full adder has shown in Fig.1(c) implements logic expressions given in (1) and (2) using 4-transistor SER XNOR, 4-transistor ground less XNOR and 2-to-1 multiplexer. Full adder 9B is can be designed from full adder 9A by interchanging the inputs of 4-transistor ground less XNOR [10]-[12].

10 transistors full adder's 13A and 9B have better critical delay than the 10 transistors SERF full adder in all loading condition. A transistor–level implementation for 10 transistor full adder 13A is shown in Fig.1 (d).

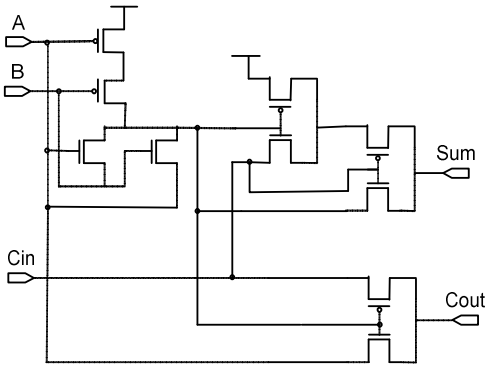
For the implementation of various 10 transistors full adder circuits we required either 4 transistors XOR circuit or 4 transistor XNOR circuit and 2-to-1 multiplexer. The basic disadvantage of the 10 transistors SERF, 9A, 9B and 13A full adders are suffering from the threshold- voltage loss of the pass

transistors. They all have double threshold losses in full adder output terminals. This problem usually prevents the full adder design from operating in low supply voltage or cascading directly without extra buffering. The lowest possible power supply is limited to 2 $V_{Tn} + V_{Tp}$ where V_{Tn} and V_{Tp} are the threshold voltages of NMOS and PMOS respectively [10]-[12].

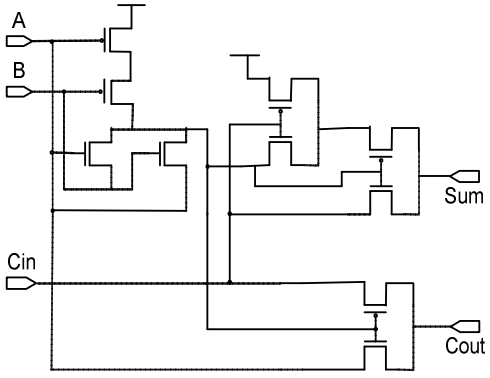
Because of the double threshold loss problem, the 10 transistor based circuits, lacking proper driving capabilities in cascaded operations, take much longer time to accomplish the computation, so they have low speed of operation.



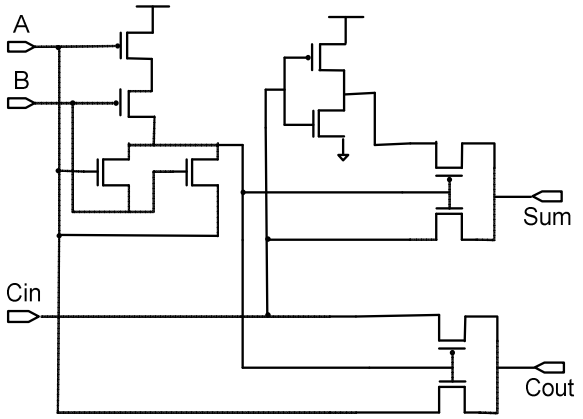
(a) SERF Adder



(b) Full Adder 9A



(c) Full Adder 9B



(d) Full adder 13A

Fig 1: 10 transistors full adder circuits

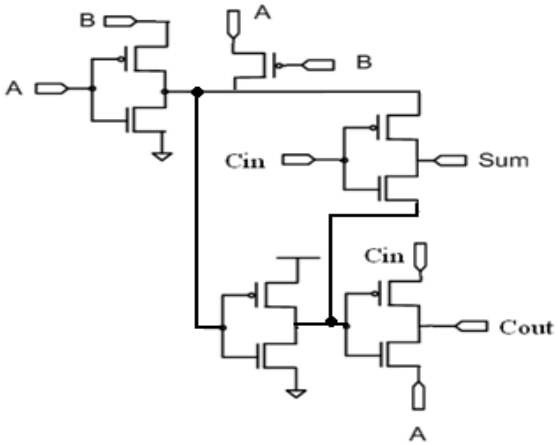
2. PPROPSED FULL ADDER CIRCUITS

The proposed 9 transistors full adder circuits are shown in Fig.2. These use a total of 9 transistors for the implementation of logic expressions (3) and (4).

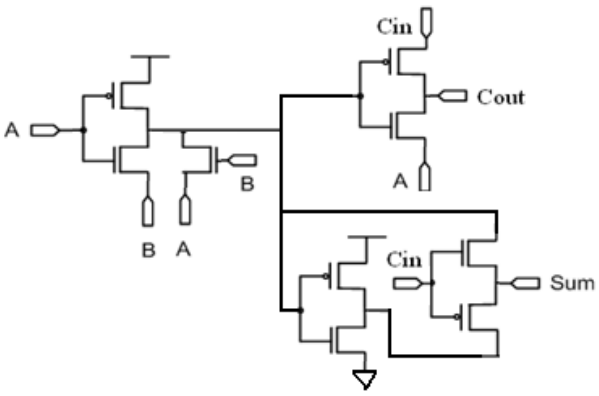
$$Sum = (A\overline{\oplus}B)C_{in} + (A \oplus B)\overline{C_{in}} \tag{3}$$

$$C_{out} = (A \oplus B)C_{in} + (A\overline{\oplus}B)A \tag{4}$$

The implementation of proposed full adder circuits required either 3 transistors XOR circuit or 3 transistors XNOR circuit, an inverter circuit and 2-to-1 multiplexer. 3 transistor XNOR circuit output is used to control 2-to-1 multiplexer circuit whose output is output carry of full adder circuit and input carry is used to control second 2-to-1 multiplexer circuit whose output is sum of full adder circuit. A transistor–level implementation for 9 transistors proposed full adder circuit-I and proposed full adder circuit-II is shown in Fig.2 (a) and Fig. 2(b) respectively.



(a) Proposed full adder circuit-I



(b) Proposed full adder circuit-II

Fig 2: Proposed 9 transistors full adder circuits

3. SIMULATION RESULTS AND DISCUSSION

Proposed full adder circuits and all reported circuits are simulated in Cadence VIRTUOSO environment using UMC 0.18 µm CMOS process technology and supply voltage of 1.8V. To perform a comparative study of performances of various full adder circuits, we need to apply the same input test pattern to all of them. The input test pattern we have used consists of the three input signals, A**,** B, and C_{IN}, and these signals are square waves of equal on and off times as shown in Fig.3.

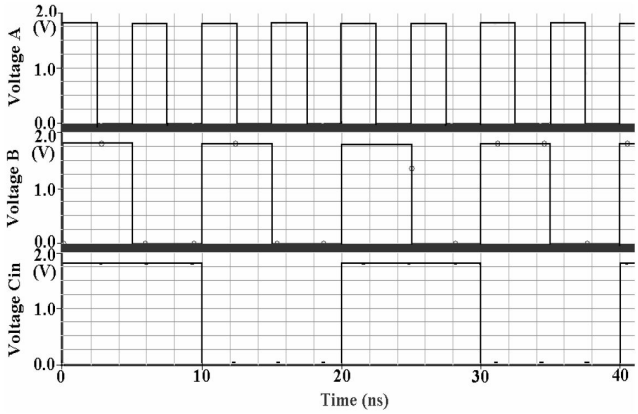


Fig 3: Input test pattern

Among the three inputs of a full adder (A, B, C_{IN}), inputs A and B are assumed to be perfect and might not be degraded due to the threshold voltage loss i.e. V_{IH} and V_{IL} for inputs A and B are V_{DD} and ground respectively. However input carry is drawn from the output carry of another full adder so it might be degraded due to threshold voltage loss.

Some frequently used architecture, such as Ripple Carry Adder, Carry Skip Adder, Carry Save Adder and Carry Select Adder are made up of chains of same Full Adders, each of which has its carry output connected to the carry input of the following one so, unless the carry out of the preceding stage is evaluated, sum of the next stage is not determined. Thus, enhancing its performance is critical for enhancing the overall module performance [13]-[14]. Therefore, for performance comparison of various full adder circuits we consider delay between input carry and output carry as an important factor.

Power consumption and delay are yardsticks for the performance of CMOS circuits. Another important standard for CMOS circuits is Power-Delay product (PDP). This parameter is applied often in testing characteristics of CMOS circuits. Since, in many cases, requirements of low power and high speed cannot be accomplished simultaneously, comparisons only using these two metrics may become problematical. Therefore, for performance comparison of various full adder circuits we consider delay between input carry and output carry, average power consumption and power delay product (PDP) as an important factors.

The comparative performance of various full adder circuits is given in Table 1.

Table 1. Comparative Performance of Various Full adder Circuits at 1.8V

Full Adder Circuit	Delay in sec	Average Power Consumption in µW	Threshold Voltage loss at Output terminals
SERF	$3.727*10^{-11}$	4.94	$V_{DD} - 2V_T$
9A	$3.632*10^{-11}$	5.904	$V_{DD} - 2V_T$
9B	$5.423*10^{-11}$	5.486	$V_{DD} - 2V_T$
13A	$3.542*10^{-11}$	5.560	$V_{DD} - 2V_T$
Proposed Adder-I	$2.191*10^{-11}$	4.065	$V_{DD} - V_T$
Proposed Adder-II	$2.88*10^{-11}$	1.850	$V_{DD} - V_T$

As shown in Table 1, the 10 transistors SERF, 9A, 9B, and 13A full adders are suffering from the threshold- voltage loss of the pass transistors. They all have double threshold losses in full adder sum and carry outputs. This problem usually prevents these full adder circuits from operating in low supply voltage or cascading directly without extra buffering. Because of the double threshold loss problem, the SERF, 9A, 9B, and 13A full adder circuits, lacking proper driving capabilities in cascaded operations, take much longer time to accomplish the computation, so they have low speed of operation. While the two proposed full adder circuits encounters only one threshold voltage loss in full adder carry and sum outputs.

The overall PDP for the proposed circuit-I have been improved by 52% to 72% at the supply voltage of 1.8V when compared with the various reported full adder circuits and for proposed circuit-II it is improved by 72% to 82% at a supply voltage of 1.8V. Graphical comparison of PDP of various full adder circuits is shown in Fig. 4.

Energy delay product (EDP) is equal to the product of worst case delay and PDP. Proposed full adder circuit shows better EDP as compared to various reported full adder circuits as shown in Fig. 5.

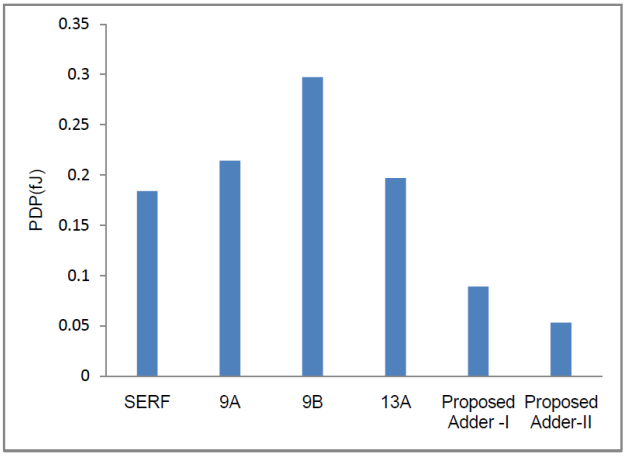


Fig 4: Comparison of PDP of Different Full Adders

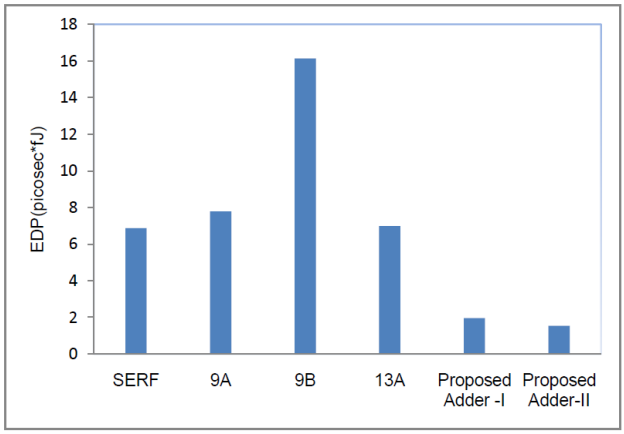


Fig 5: Comparison of EDP of Different Full Adders

4. CONCLUSION

In this paper, we consider various full adder configurations and compare their performance in Cadence VIRTUOSO environment. The proposed circuits have been tested in 0.18 µm CMOS technology and operate successfully at different supply voltages. Based on simulation results, it is conclude that the proposed circuits have good signal level, consume less power and have high speed compare to all other designs at low supply voltage. The proposed design-II is 19% to 47% faster than the 10 transistors full adder circuits and 6% to 67% less power consumption as compared to various 10 transistors full adder circuits.

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