Behavior and Mathematical Modeling of PLL at 450MHz

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ABSTRACT
Phase Lock Loop (PLL) is major analog circuit used for many different communication applications such as frequency synthesizer, radio, computer, clock generation and recovery, global positioning system etc. Therefore, the selection criteria for the desired PLL design is a critical and time consuming issue. This paper applies selection of proposed type of PLL for the desired application and analysis of third order PLL. The MATLAB Simulink tool is used for parameter selection and verification. The performance of PLL is tested and calculated for parameters like lock time, lock range, Bandwidth.

General Terms
Simulation, Design, Verification.

Keywords
CAD, EDA tools, Simulink VCO, PLL Baseband PLL, Charge pump PLL, literalized PLL

1. INTRODUCTION
Phase locked loop is an excellent research topic as it covers many disciplines of electrical engineering such as Communication Theory, Control Theory, Signal Analysis, Noise Characterization, Design with transistors and op-Amps, Digital Circuit design and non-linear circuit analysis. Later on with the development of integrated circuits, it found uses in many other applications. The first PLL ICs came in existence around 1965, and was built using purely analog devices. Recent advances in integrated circuit design techniques have led to an increased use of the PLL as it has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single Chip i.e SoC[1] [13]. MATLAB simulink[15] is effective tool to get prior idea about PLL parameters to fulfill requirements before actual chip design. MATLAB simulink is effective tool to to get prior idea about PLL parameters to fulfill requirements before actual chip design .

Phase Locked Loops are used in almost every communication system. Some of its uses include recovering clock from digital data signals[3], performing frequency, phase modulation and demodulation, recovering the carrier from satellite transmission signals and as a frequency synthesizer[2]. There are many designs in communication that require frequency synthesizer to generate a range of frequencies; such as cordless telephones, mobile radios and other wireless products. The accuracy of the required frequencies is very important in these designs as the performance is based on this parameter [1] [13] [4].

A Phase Locked Loop is a feedback control circuit. As the name suggests, the phase locked loop operates by trying to lock to the phase of a very accurate input signal through the use of its negative feedback path. A basic form of a PLL consists of three fundamental functional blocks namely Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO).The block diagram of PLL is shown in the figure 1.The different types of PLL can broadly categories as Analog PLL, Digital PLL and Hybrid PLL.

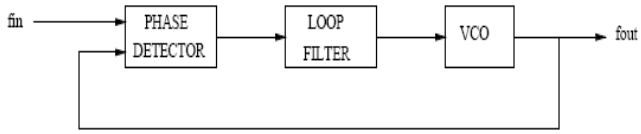

Figure 1. The block diagram of PLL

PLLs have several unique characteristics when viewed from a control systems perspective. First of all their correct operation depends on the fact that they are nonlinear. The loop does not exist without the presence of two nonlinear devices, namely the phase-detector and VCO[3]. Therefore in this work the variation in different parameters for PLL are tested against VCO sensitivity, Loop filter transfer function for particular application.

The remainder of the paper is organized as follows. In Section 2, the basic of Linearized model of PLL is explained. The equation for lock time (T_L), Bandwidth (BW) and lock range (Δw_L) is listed. In section 3,the frame for PLL design using Matlab/Simulink is explained. In section 4, the obtained results were compared with theoretical calculation.

2. LINEARIZED PHASE DOMAIN MODEL FOR PLL
The generalized loop response for the higher ordered PLL can be written as equation (1)[1], [2], [14]

$$\frac{\theta_0}{\theta_i} = \frac{K_p K_v F\ s}{s + K_p K_v F\ s} \quad \text{..... (1)}$$

Where,

θ_0 = the output phase in radians

θ_i = the input phase in radians

K_p =the phase detector gain in volts per radian

K_v = the VCO gain in radians per volt-second

$F\ s$ = the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by changing different types of loop filters then the order of PLL is $n+1$ where n order of the loop filter.

The simplest filter is a one-pole RC circuit. The loop transfer function in this case is given a equation 2.

$$F\ s = \frac{1}{1+sRC} \quad \text{..... (2)}$$

The loop response for 2nd order PLL can be found out using eq. (2), (3).

$$\frac{\theta_0}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}} \quad \text{..... (3)}$$

Comparing the equation 3 with standard transfer function equation of second order filter we get,

$$\xi = \frac{1}{2\sqrt{K_p K_v RC}} \quad \text{..... (4)}$$

$$\omega_n = \sqrt{K_p K_v / RC} \quad \text{..... (5)}$$

Where,

RC =Time constant in sec.

ξ = damping ratio

ω_n = natural frequency

For sinusoidal phase detector K_P is ½ of peak to peak voltage of PD output [4]

Using equation (3),(4),(5) we get ,

Lock time , $T_L = 2\Pi/\omega_n$ .....(6)

Lock range , $\Delta w_L = \Pi \xi \omega_n$ .....(7)

Bandwidth , $BW = \omega_n \left[1 - 2\xi^2 + \sqrt{2 - 4\xi^2 + 4\xi^4}\right]^{1/2}$ ..(8)

The corresponding values for lock time, Lock range, Bandwidth is calculated for different types of PLL, Baseband PLL, Charged Pump PLL[2].The pump current I_p and selection of the capacitor C for filter design (mostly in nF) is an important design factor to be considered while designing charged pump PLL. Generally value of Ip is 100 μA to 1 mA][2] [7] [4].

Equation(9),(10) obtained by comparing closed loop transfer function of second order PLL and standard second order PLL equation in terms of ω_n, ξ

$$\omega_n = \sqrt{\frac{I_p Kvco}{2\Pi C_p}} \quad \text{.....(9)}$$

$$\xi = R_p \sqrt{\frac{I_p c_p Kvco}{2\Pi}} \quad \text{.....(10)}$$

As expected, if Rp=0, then ζ =0. With complex poles, the decay time constant is given by equation (11) as

$$\frac{1}{\xi\omega_n} = \frac{4\Pi}{R_p I_p K_{vco}} \quad \text{.....(11)}$$

As seen from the closed loop transfer function of second order PLL equations (13), (14) if we decrease the $I_p * K_{vco}$,the gain crossover frequency decreases (or shifts toward the origin), degrading the phase margin. Since the charge pump drives the series combination of R_p and C_p , each time a current is injected into the loop filter, the control voltage experiences a large jump. Even in the locked condition, mismatches between I_{UP} and I_{DOWN} and the charge pump injection and clock feed through of S1 and S2 introduce voltage jump in V_{CONT} as shown in the figure 3.

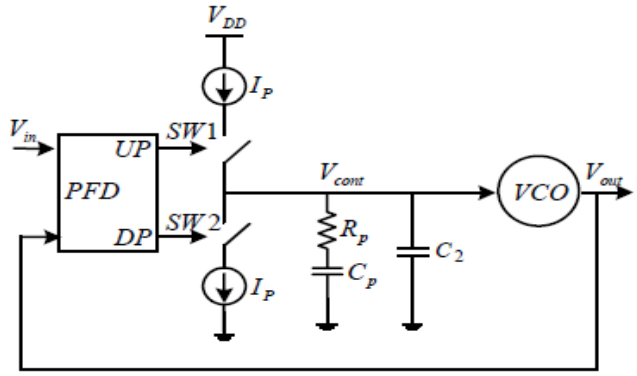

Figure.2. Structure of third order charge pump PLL

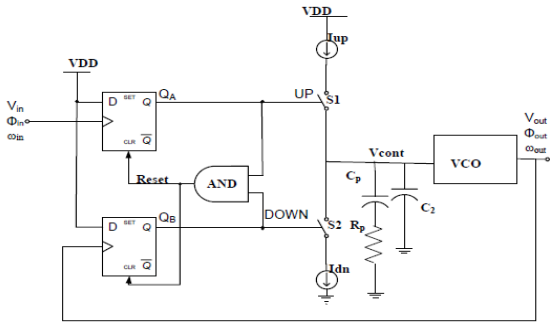

Figure. 3. Addition of C2 to improve stability

Design and analysis of third order PLL is important as higher order design are concerns with system stability designed for wide applications.Trasfer function for second order filter for charge pump PLL is given by equation (12) . The structure of third order charge pump PLL and System model of charge pump PLL block diagram shown in figure 2,figure 4 respectively.

Transfer function of loop filter is given by equation (12)

$$Rp + 1/C_p S\} // 1/C_2 S \quad \text{.....(12)}$$

The open loop and closed loop transfer function is given by equations (12), (13) .

$$G_0(s)=\frac{\frac{I_pK_{vco}}{2\pi}(sRC_1+1)}{S^3RC_1C_2+S^2\ C_1+c_2} \quad \text{..... (13)}$$

$$G_c(s)=\frac{\frac{sI_pK_{vco}R}{2\Pi}+\frac{I_pK_{vco}}{2\Pi C_1}}{s^3mRC_1+\frac{sI_pK_{vco}R}{2\Pi}+\frac{I_pK_{vco}}{2\Pi C_1}} \quad \text{..... (14)}$$

where I_p is the current of charge pump,

K_{vco} is the VCO gain constant

m= $\frac{c_2}{c_1}$ is the capacitance ratio.

Usually, C2 is much smaller than C1 (m«1). Comparing equation (13) with equation (14) will get ξ, ω_n and m.

$$G_c(s)=\frac{2\xi\omega_n s+\omega^2}{m\frac{2\xi}{\omega_n}s^3+(m+1)s^2+{\omega_n}^2} \quad \text{..... (15)}$$

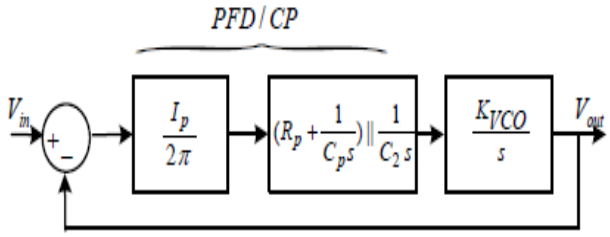

Figure 4.System model of charge pump PLL block diagram

3. FRAME WORK FOR PLL DESIGN

The set up arrangement done for PLL parameter measurement is shown in the figure 2. The similar set up is has been designed for Linearized Baseband PLL, Charged Pump PLL. The set up for Baseband PLL is shown in the figure 5.Similar set up is done for Linearized Baseband PLL, Charged Pump PLL.

3.1 Setup for PLL Simulation in Simulink

The input provided in set up is order coefficient of Loop filter. For e.g., using the transfer function of Loop filter incorporated in automated program written in Matlab which guides to find the input to find the proper range of input applied to the set up assembly to get desired output. Similarly for other input parameters Like, VCO gain in Hz/volts and quiescent frequency were found out.

For analysis of third order PLL setup used is almost same as second order PLL ,I/P for assemble are TF of loop filter ,Kvco, quiescent frequency of VCO.

3.2 Measurement of PLL parameters

The simulation is done in Simulink/Matlab 2009b on Intel processor core 2 Duo processor@ 2.93 GHz with 1.96GBRAM The simulated results for filter output ,phase detector output and VCO outputs can seen in real time using scope in Simulink.

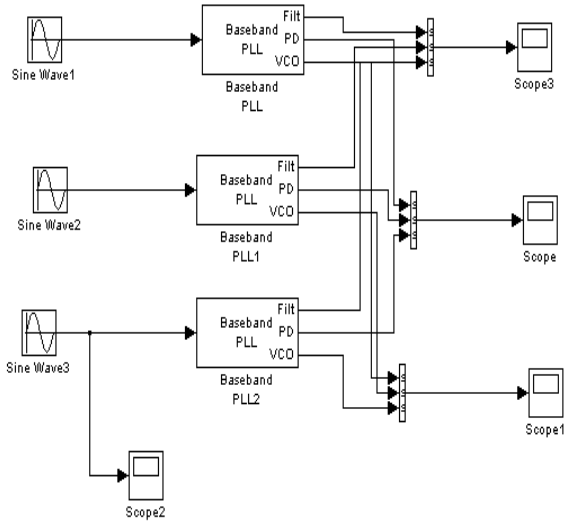

Figure 5. Setup for measurement of PLL parameters in Simulink

The obtained VCO output, filter output ,Phase detector output for Charge pump PLL is shown in figure 7, figure 8 and figure 9 respectively.similarly filter output (control signal),PD output and reference signal & VCO output shown in figure (10,11,12) respectively. These obtained data at least 5000 samples per result were stored in workspace. The peak value i. e $A1$ and next peak value $A2$ are found out from these samples using program written in Matlab [9],[10]. Using these retrieved values ξ and ω_n was found out using the formulae figure 6. [4]. The automated program files guides to find calculated and observed value for given RC time constant.

Figure 6. Measurement of PLL

$$\xi=\frac{\ln\ A1/A2}{\sqrt{\Pi^2+\left[\ln\ A1/A2\ ^2\right]}} \quad \text{.....(11)}$$

$$\omega_n=\frac{2\Pi}{T\sqrt{1-\xi^2}} \quad \text{..... (12)}$$

Where,

$A1$ =First maximum peak amplitude

$A2$ = First minimum peak amplitude

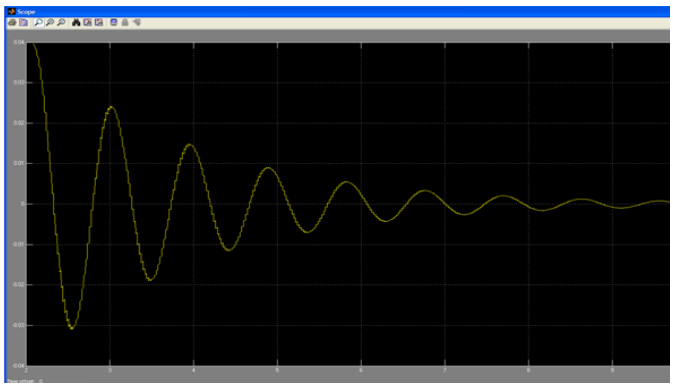

Figure 7. Charge pump PLL filter output

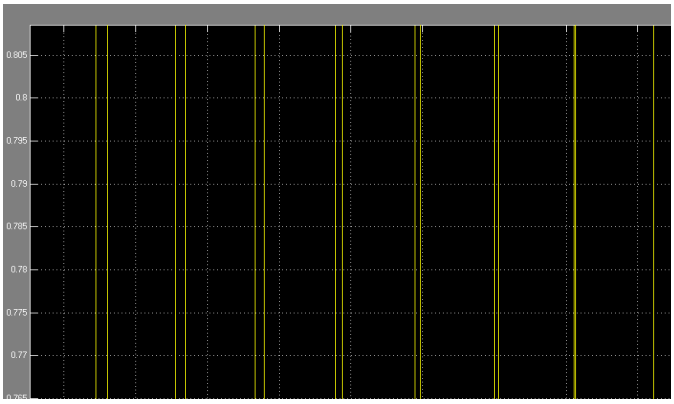

Figure 8. Charge pump PLL Phase detector output

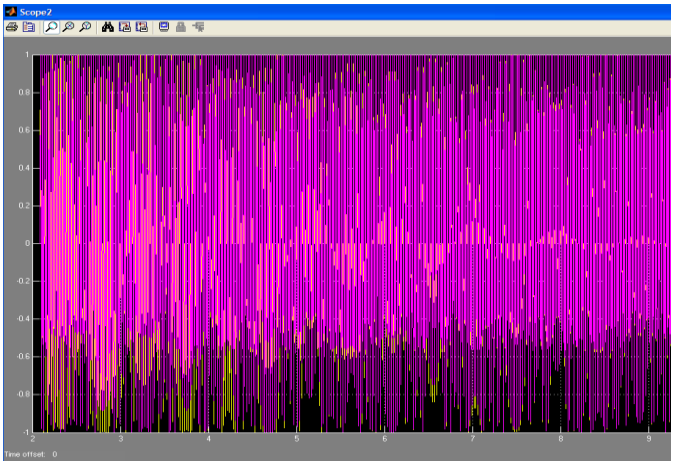

Figure 9. Charge pump PLL VCO output and input signal

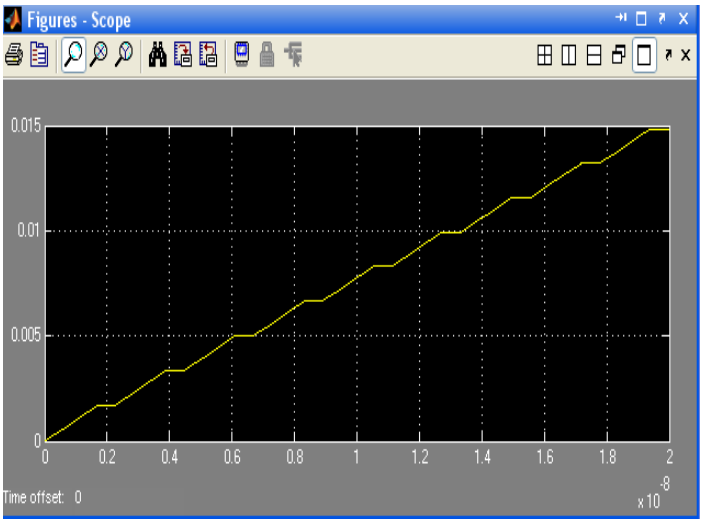

Figure 10. Third order Charge pump PLL filter output

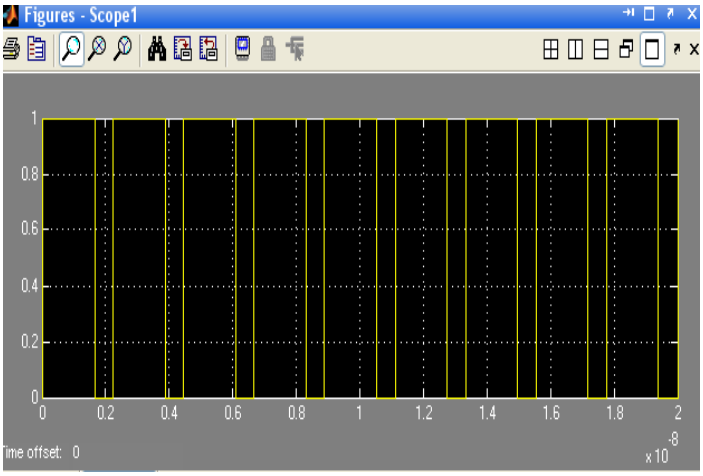

Figure 11. Third order Charge pump PLL Phase detector output

Output of PD and filter output indicate that $\Delta\theta = 90$.Bode plot of open loop and closed loop third order PLL shown in figure 14,15respectively. The step response of third order system is shown in figure 13 shows.

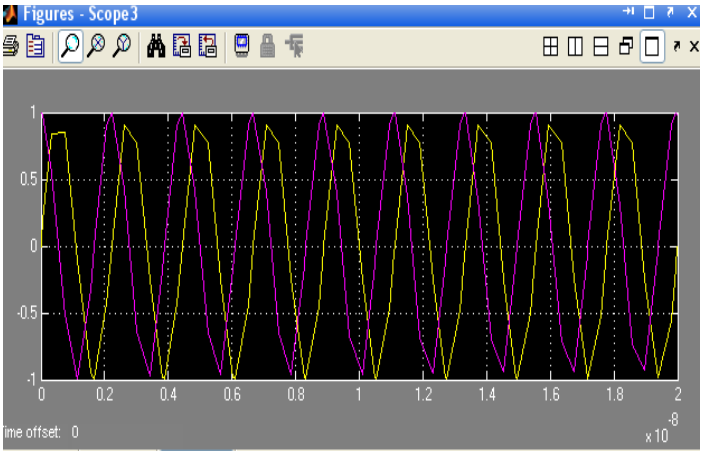

Figure 12. Third order Charge pump PLL VCO output and input signal

3.3 Automated program for third order Charge pump PLL

Automated program used for design of third order Charge pump PLL is written in MATLAB. These This program guides user to find the component values for specific parameter of PLL.

[cap res] = pll_synth_2nd_order(ipump, vco_sensitivity, fout, fcomp, bandwidth, pm)

Where,

ipump=chargr pump current

Kpd=(ipump/2)/pi; % phase detector gain

Kvco = vco_sensitivity*2*pi; % vco gain

omega = 2*pi* bandwidth; % open loop bandwidth in radians/sec

Then after finding loop parameters using Ao,T1,T2 will get PLL design component values,Example is shown as following example.

[cap res] =

pll_synth_2nd_order(100e-6,166.948e6,450e6,100e3,200e6,60)

cap =

1.0e-016 *

0.0630 0.8138 0 0

res = 1.0e+007 *

3.6492 0 0

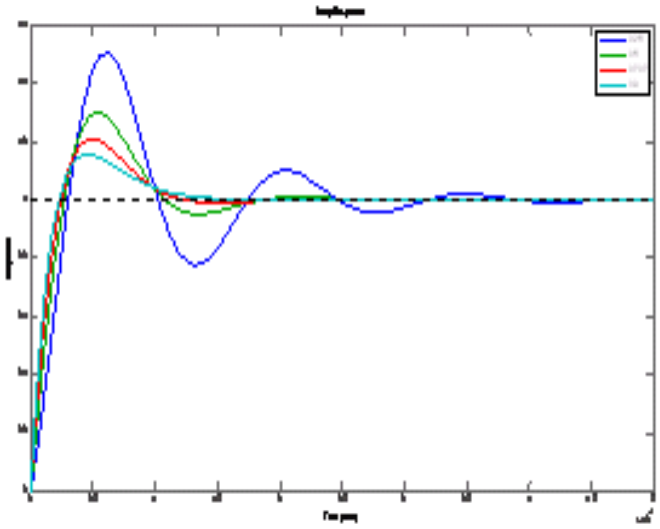

Figure 13. Step response for different values of ζ of Charge pump PLL

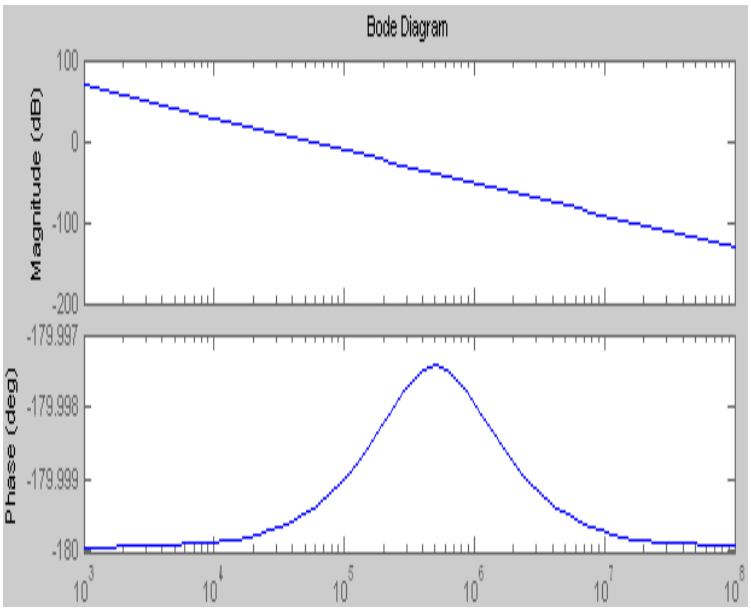

Figure 14. Open loop Bode plot of third order CPPLL

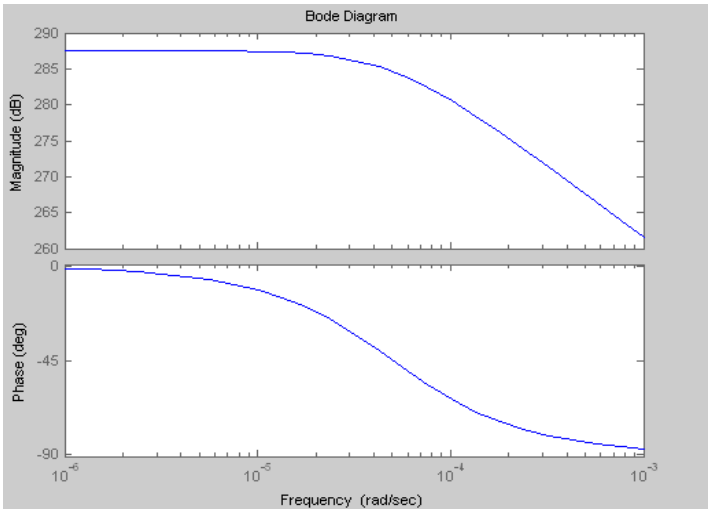

Figure 15. Closed loop Bode plot of third order CPPLL

4. RESULT AND DISSCUSSION

For the different type of PLL, the comparative study of obtained results of PLL for parameter such as setting time (sec to msec), Bandwidth (Hz to MHz),Lock range(Hz-KHz) is shown in figure 15-22.

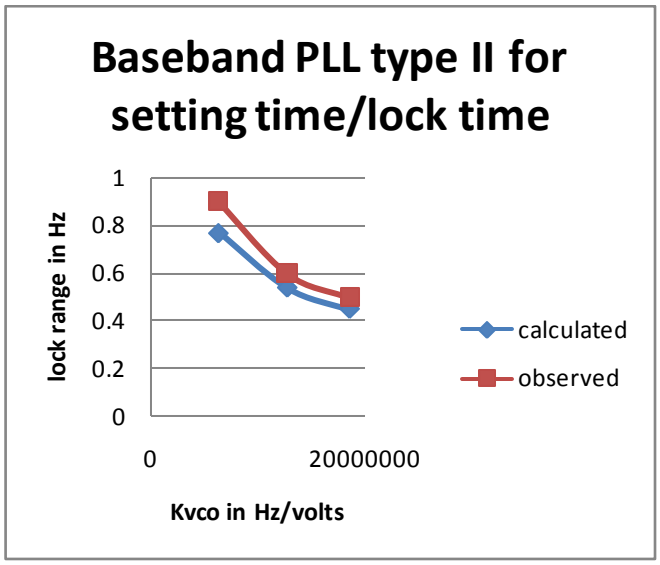

Figure 15. Baseband PLL TYPE II for lock time

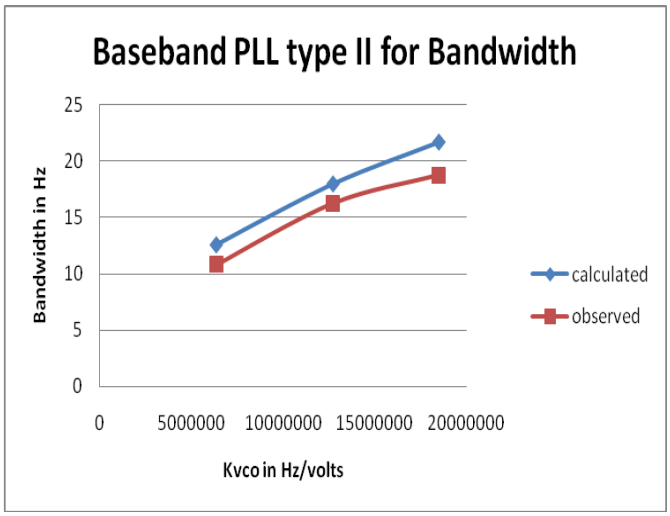

Figure 16. Baseband PLL TYPE II for Bandwidth

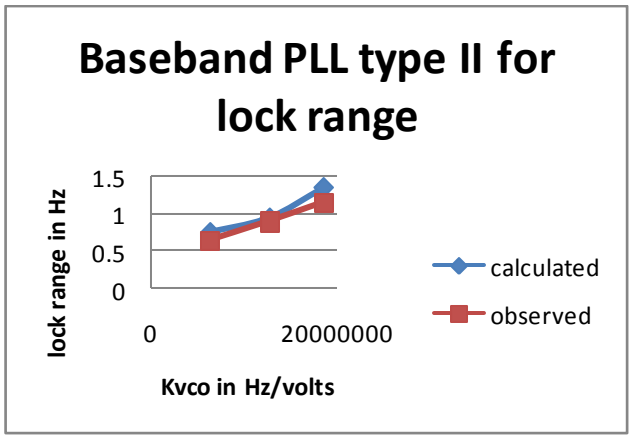

Figure 17. Baseband PLL TYPE II for lock range

From figure15-17 ,It can be found out that Baseband PLL can be used for narrow BW apllications such as GPS its around (0-10Hz) since the drawback is as Kvco increases setting time increasestherefore selection RC time constant is acritical issue. and its lock range is small in range of few Hz.

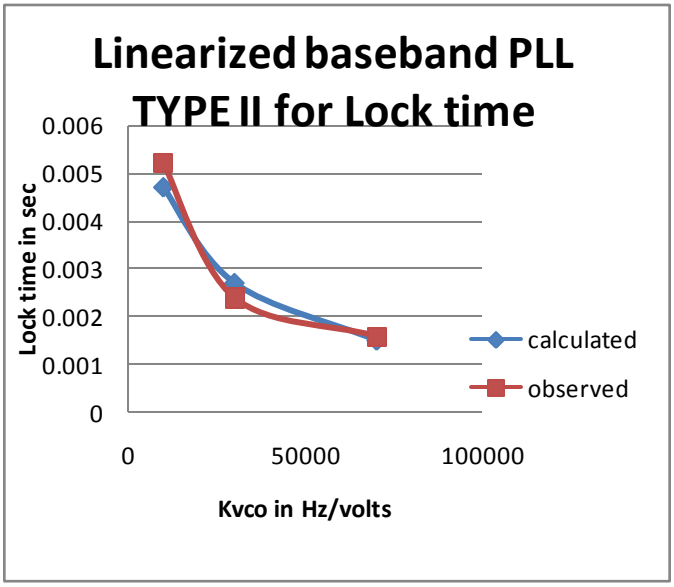

Figure 18.Linearized Baseband PLL TYPE II for lock time

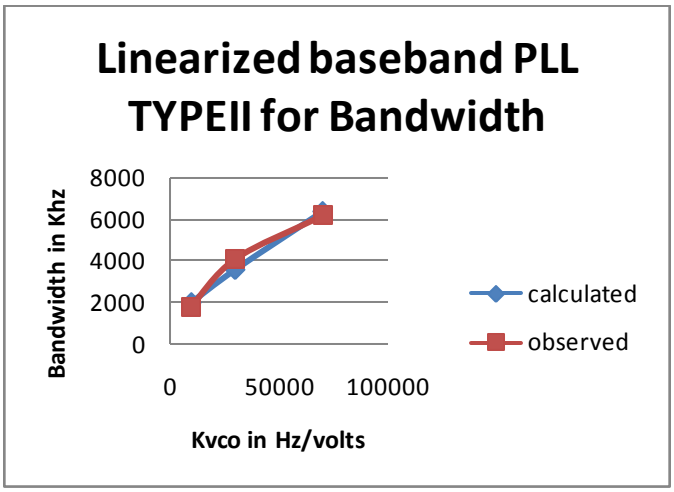

Figure 19.Linearized Baseband PLL TYPE II for Bandwidth

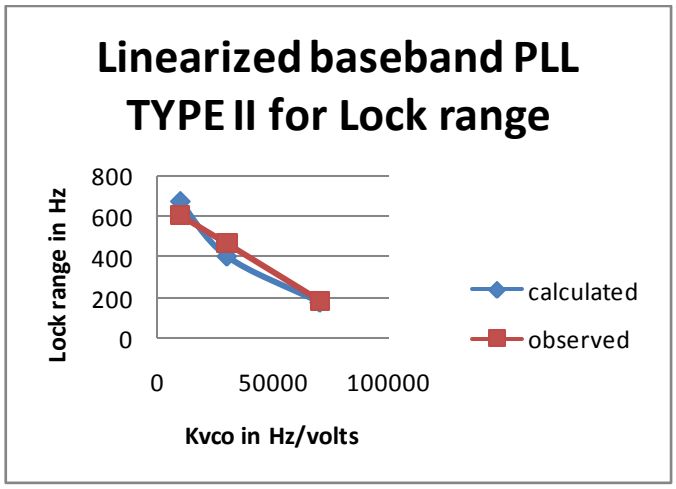

Figure 20.Linearized Baseband PLL TYPE II for lockrange

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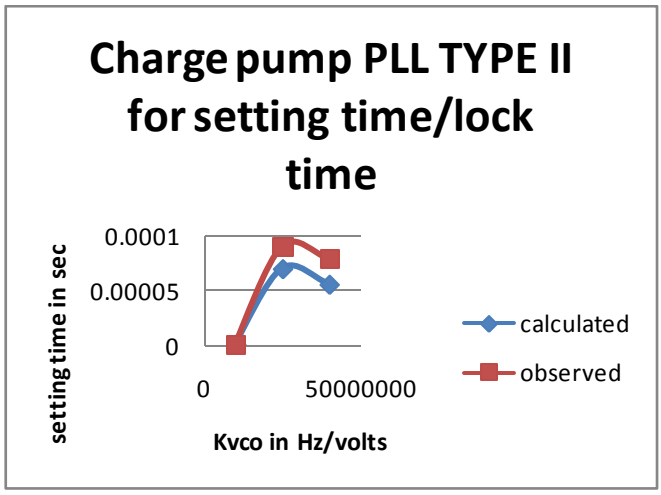

Figure 21.Charge pump PLL TYPE II for lock time

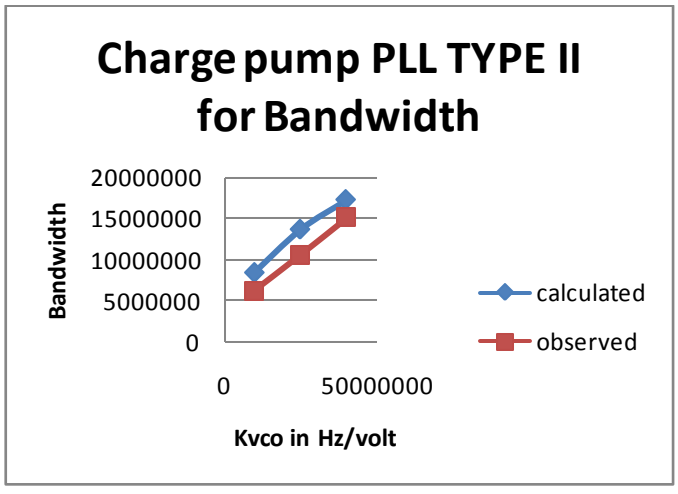

Figure 22.Charge pump PLL TYPE II for Bandwidth

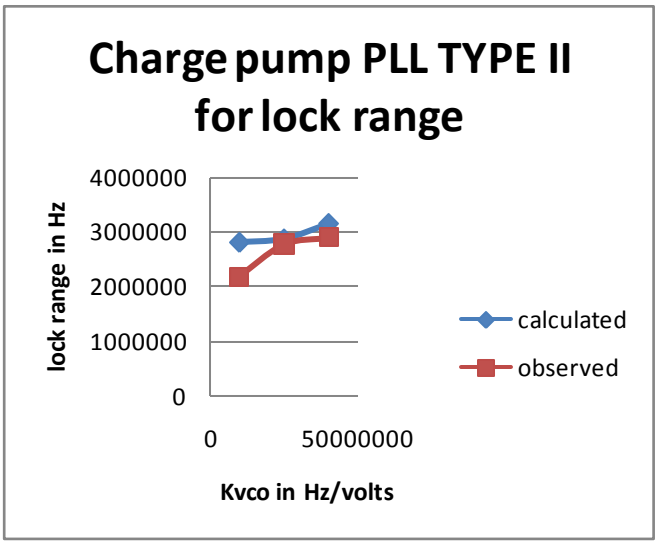

Figure 23.Charge pump PLL TYPE II for lock range

Parameter	ξ=0.707	ξ=0.9
Settling time	125.7nsec	98.76nsec
Overshoot%	1.18%	0.000035%
m	0.000083	0.00001
Loop gain	4.575Mhz	7.9056Ghz

From the graph 18-20,It was found that for Linearized PLL K_{VCO} inreases its lock range decreases drastically. The linearized model and the nonlinearized model differ in that the linearized model uses the approximation $\sin(\Delta\theta(t)) \cong \Delta\theta(t)$ to simplify the computations. This approximation is close when $\Delta\theta(t)$ is near zero. Thus, instead of using the input signal and the VCO output signal directly, the linearized PLL model uses only their phases.

From the graph 21-23,It was observed that for Charge pump PLL we get wider Bandwidth [9],[11],[12],faster setting time and large lock range [13].The comparative result table for baseband, Lineaized baseband and chgre pump PLL is listed in table 3.

Table 1.Simulation results for 0.707 and 0.9

Table 1 shows design of PLL at critical phase margin, and comparative effect for $\xi = 0.707$ and $\xi = 0.9$ .From the obtained results it can be seen that as damping factor increases the PLL setting time decreases ie faster setting ,as well as overshoot also decreases. Table 2 shows the list of componetnt valuecs obtained by using automated program.

Table 2. Design component values

Damping factor	C_1	C_2	R
$\xi = 0.707$	0.1 μf	83.03Pf	24kΩ
$\xi = 0.9$	2Pf	0.00002Pf	20kΩ

Table31. Comparative result table for all types of PLL

PLL TYPE	Kvco in Hz/volts	Lock time Cal	Lock time Obs	Lock Range Cal	Lock Range Obs	Bandwidth Cal	Bandwidth obs
Baseband PLL	6.36 KHz/volts	0.75 sec	0.9 sec	0.75 Hz	0.65 Hz	12.5Hz	10.8Hz
	12.7 k Hz/volts	0.54 sec	0.60 sec	0.9393Hz	0.9394Hz	17.96 Hz	16.24 Hz
	18.5K Hz/volts	0.45 sec	0.52 sec	1.33 Hz	1.145 Hz	21.66 Hz	18.74 Hz
Charge pump PLL	100 Mhz/volts	1.13 µsec	1.5µsec	2.83 MHz	2.19 MHz	8.6 MHz	6.28 MHz
	250 Mhz/volts	70.4 µsec	90.5 µsec	2.89 MHz	2.78 MHz	138 MHz	152 MHz
	400 Mhz/volts	56.1 µsec	79.3 µsec	3.17 MHz	2.9 MHz	173 MHz	152 MHz
Linearized baseband PLL	10 Khz/volts	4.7 msec	5.2 msec	671.2 Hz	601.98Hz	2.0397 KHz	1.8293 KHz
	30 Khz/volts	2.7 msec	2.4 msec	405.2 Hz	464.97Hz	3.5922 KHz	4.119 KHz
	70 Khz/volts	1.5 msec	1.6 msec	186.0 Hz	182.0765Hz	6.3493 KHz	6.213 KHz

5. CONCULSION

The effect on parameters of second order PLL designed at 450Mhz is discussed in this work. Simulation results show that ξ and ω_n affect the behaviour of different PLL types. From the observed results, it is found out that, Linearized PLL is not used widely in communication applications due to constraint of smaller lock range for higher value of $K_{VCO.}$ The use Baseband PLL is restricted to for narrow BW apllications such as GPS systems in mobile communication whereas, Charge pump PLLcan be widely used for many communication application due to its advantage as it provides wider Bandwidth, less setting time and wider lock range.

The novel method for analysis and simulation of third order PLL is proposed. This method is an efficient method which helps to find stability of system with good precision in designed parameters. In future, we proposed to analysis of PLL in presence of noise and to achieve minimum phase noise.

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