

# Study of Variation of THD in a Diode Clamped Multilevel Inverter with respect to Modulation Index and Control Strategy

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## ABSTRACT

Due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. In this paper, a Diode Clamped Multilevel Inverter is controlled with Sinusoidal PWM, Third Harmonic Injection PWM and Sixty degrees PWM and the variation of Total Harmonic Distortion in their outputs are observed. Also, a Diode Clamped inverter is controlled by Sinusoidal PWM technique and by varying the modulation index, variation of Total Harmonic Distortion is observed.

## General Terms

Multilevel Inverter, Pulse Width Modulation.

## Keywords

Diode Clamped Multilevel Inverter, Sinusoidal PWM, Third Harmonic Injection PWM, Sixty Degree PWM, Total Harmonic Distortion.

## 1. INTRODUCTION

Multilevel Inverter uses an array of series switching devices to perform power conversion in incremental steps of voltage by synthesizing the staircase voltage from several levels of DC capacitor voltages [1]. The multilevel voltage source inverter is recently used in many industrial applications AC power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. Multilevel inverters can improve the voltage quality and reduce the voltage stress on the power electronic devices.

### 1.1 MULTILEVEL INVERTERS

It may be easier to produce a high power, high-voltage inverter with the multilevel structure because of the ways in which device voltage stresses are controlled. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformers or series connected synchronized switching devices.

As the number of voltage levels increases, there is more decrease in harmonic content of the output voltage waveform. Multilevel inverters offer a low total harmonic distortion (THD) for output voltage, high efficiency and power factor. They have higher efficiency because the devices can be switched at a low frequency. With additional voltage levels, the voltage waveform has more free-switching angles, which can be pre-selected for harmonic elimination. The switching devices do not encounter any voltage sharing problems. For this reason, multilevel inverters can easily be applied for high-power applications, such as, large motor drives and utility supplies. The fundamental output voltage of the inverter is set by the DC bus voltage, which can be controlled through a variable DC link.

### 1.2 Multilevel Inverter Configurations

Basically, there are three kinds of multilevel inverters: (1) Diode-clamped multilevel inverter; (2) Flying-capacitor multilevel inverter; (3) Cascade multilevel inverter. All the three converters have the potential for applications in high-voltage, high-power systems, such as, static VAR generator (SVG) without voltage unbalance problems; because the SVG does not draw real power. Diode-clamped converter is most suitable for back-to-back intertie, but it would require more switching per cycle. The multilevel inverters can find potential applications in adjustable speed drives, where multilevel inverters can solve harmonic problems and also avoid possible high-frequency switching dv/dt induced motor failures. The cascaded inverter [4] uses a full bridge in each level as compared with half-bridge version for the other two types. The cascaded inverter requires the least number of components and has the potential for utility interfacing applications because of its capabilities for applying modulation and soft switching techniques.

### 1.3 Voltage Source Inverters

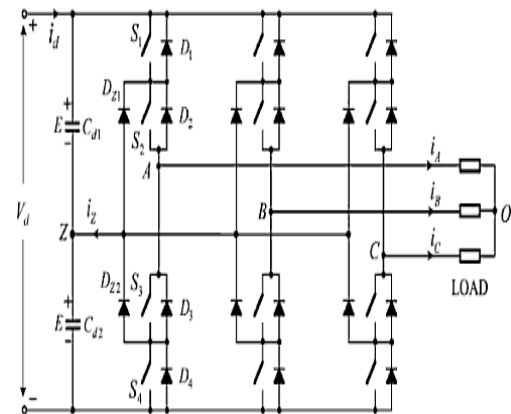
A voltage source inverter consists of a turn-off device connected in anti-parallel with a diode which has lowest reverse leakage current with the anode of turn-off device connected to the positive side of DC side. In inverter action, turn-off device will conduct and current / power flows from DC side to AC side. In rectifier action, the diode will conduct and current / power flows from AC to DC side[5]. Under inverter operation, current and voltage will be of opposite polarity and under rectifier operation they will be of same polarity. The compensation is applied at mid-point to improve the voltage regulation. For radial lines, shunt compensation is applied at the end of line to prevent voltage

instability, for dynamic voltage control, to increase transient stability and for damping of power oscillations. Mid-point of transmission line is the best location for compensator because the voltage sag for uncompensated line is maximum at the mid-point. Also, the compensation at mid-point breaks the line into equal segments, for each of which, the maximum transmittable power is the same.

### 1.4 Three Level Inverter

The three-level inverter topology is being widely used in high voltage, high power applications due to its high voltage handling and good harmonic rejection capabilities with currently available power devices. Figure 1 shows the basic circuit diagram of a three-level inverter excluding detailed snubber circuit.

It is known that the three-level inverter roughly improves by a factor of four the harmonics content compared with conventional two-level topology having the same number of devices and ratings. Various PWM techniques for control of three-level inverter have been studied, such as, modified two-level triangular carrier modulation, cost function minimizing PWM and space vector PWM.



**Fig 1: Three Level diode clamped inverter**

In the proposed configuration, a three-level diode clamped inverter is used. It is controlled by a sinusoidal pulse width modulation scheme.

An m level inverter leg requires  $2(m-1)$  switching devices and  $(m-1)(m-2)$  clamping diodes. For a three-level inverter,  $m=3$ , so it needs four switching devices and two clamping diodes per leg as shown in Figure 1.

1. For an output voltage of  $V_a = V_{dc}$ , all the upper-half switches of a-phase leg are turned ON, i.e., S1 and S2 are ON.
2. For output voltage of  $V_a = V_{dc}/2$ , only S2 and S3 are ON.
3. For output voltage of  $V_a = 0$ , all the lower-half switches of a-phase leg are turned ON, i.e., S3 and S4 are ON.

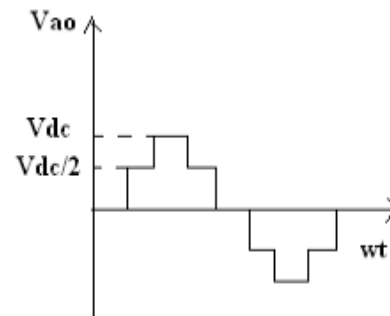
Table 1 shows the voltage levels and their corresponding switch states. State condition '1' means the switch is ON, and state '0' means the switch is OFF. It should be noticed that there are two

complementary switch pairs. These pairs for one leg of the inverter are (S1, S3) and (S2, S4).

**Table 1. Switch states for various voltages of a phase leg**

Voltage level $V_a =$	$S_{A1}$	$S_{A2}$	$S_{A3}$	$S_{A4}$
$V_{dc}$	1	1	0	0
$V_{dc}/2$	0	1	1	0
zero	0	0	1	1

Thus, if one of the complementary switch pairs is turned ON, the other of the same pair must be OFF. Two switches are always turned ON at the same time. Output voltage waveform of a three level inverter is as shown in Figure 2.



**Fig 2: Output voltage waveform of a three level inverter.**

For m-level Diode Clamped inverter, each switching device is only required to block a voltage level of  $V_{dc}/(m-1)$ . Unequal conduction duty requires different current ratings for switching devices. Therefore, if the inverter design uses the average duty cycle to find the device ratings, the upper switches may be over sized, and the lower switches may be undersized.

A diode clamped inverter is mostly used because control method is simple. Also, when the number of levels is high enough, the harmonic content is low enough to avoid the need for filters. But, it is limited by the increase in number of clamping diodes as the number of levels increases. Also, it is difficult to control the real power flow of the individual converter in multi-converter systems.

### 1.5 CONTROL STRATEGY

There are two methods of controlling the AC output voltage. In the first method, there is only one turn on, turn off per device per cycle. Here, the AC output voltage can be controlled by varying the width of the voltage pulses, and / or the amplitude of the DC bus voltage. The second method (PWM) is to have multiple pulses per half cycle, and then vary the width of the pulses to vary the amplitude of the AC voltage. In this method, lower order harmonics can be reduced. But, more pulses mean more switching losses. Therefore, the gains from the use of PWM have to be sufficient to justify an increase in switching losses. Using PWM

techniques, it is possible to control the output voltage and optimize the harmonics.

Various switching strategies can be employed to control multilevel inverter. Sinusoidal PWM technique has the advantages of real-time control, linear operation, good transient response, and a constant average switching frequency. An inherent current loop can even be added to obtain instantaneous current control. Selective harmonic elimination technique [6] can be used to eliminate certain lower order harmonics by controlling the firing pulses. But, the disadvantage of this technique is that the elimination of lower order harmonics will increase the next higher level harmonics. Harmonic loss depends on rms ripple current. If minimizing harmonic loss is the main concern, then minimum rms ripple current technique can be used.

If load neutral is connected to the center tap of the DC supply, all the three half bridges operate independently. If neutral is isolated, then the phases interact.

Space vector modulation technique considers this interaction of phases and optimizes the harmonic content[7]. This method involves look up tables or mathematical calculations of switching states, which is easier for digital implementation by a single chip microprocessor[8]. But, the main drawback is that the complexity increases with increase in number of levels. In Hysteresis Band Current Controlled PWM technique, the actual current continuously tracks a command current within a hysteresis band. This method has gained popularity because of its simplicity, fast transient response, direct limiting of device peak current and practical insensitivity of DC link voltage that permits a lower filter capacitor. But, the PWM frequency is not constant, and as a result, non-optimum harmonic ripple is generated. Fundamental current suffers a phase lag that increases at higher frequency. Sigma-delta modulation is yet another technique; where in, variable frequency variable voltage sinusoidal output can be generated.

### 1.6 SINUSOIDAL PWM

In this scheme, three sinusoidal reference waves each shifted by  $120^\circ$  are used. A triangular carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase. Magnitude and frequency of resultant wave is dependent on the magnitude and frequency of carrier wave. In the present configuration, modulation index (which is a ratio of peak value of reference wave to peak value of carrier wave) is varied in the range 0.7-0.95. Reference wave, carrier wave and resultant pulses that are generated can be viewed in Figure 3.

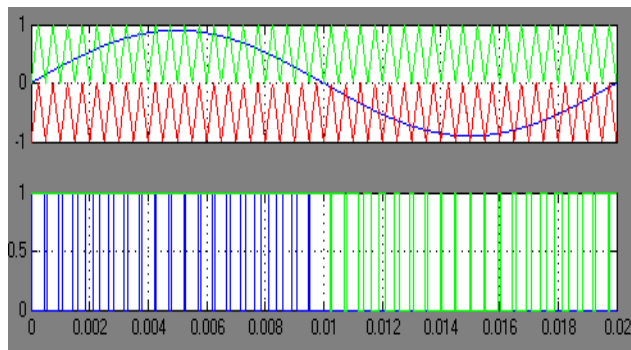


Fig 3: Sinusoidal PWM Technique

### 1.7 Third Harmonic Injection PWM

In this technique, a third harmonic component is superimposed on the fundamental. The addition of third harmonic makes it possible to increase the maximum amplitude of fundamental in the reference and in the output voltages [2].

Third harmonic technique is preferred in three-phase applications, since cancellation of third harmonic components and better utilization of DC supply can be achieved. Harmonic elimination techniques, which are suitable for fixed output voltage, increase the order of harmonics and reduce the size of output filter. But, these advantages should be weighed against increase in switching losses of power devices and iron losses in transformer due to high harmonic frequencies. It is not always necessary to eliminate triplen harmonics, which are not normally present in three-phase connections. So, in three-phase inverters, it is preferable to eliminate fifth, seventh and eleventh harmonics of output voltages, so that the lowest order harmonic will be thirteenth [3]. Firing pulses generation with third harmonic injection PWM method is as shown in Figure 4.

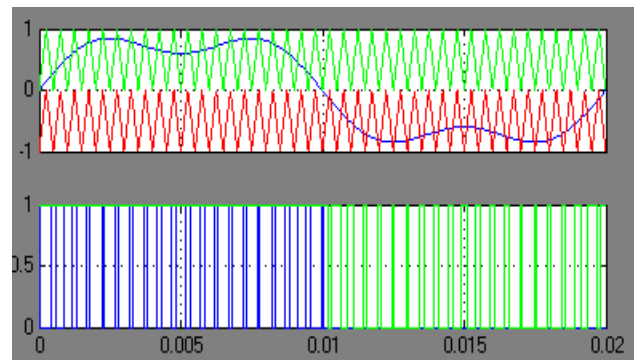


Fig 4: Third Harmonic Injection PWM technique

### 1.8 60 degrees PWM

This method is almost similar to sinusoidal PWM except that the modulating sine wave is flat topped for a period of 60 degrees in each half cycle. 60 degrees PWM technique is as shown in Figure 5.

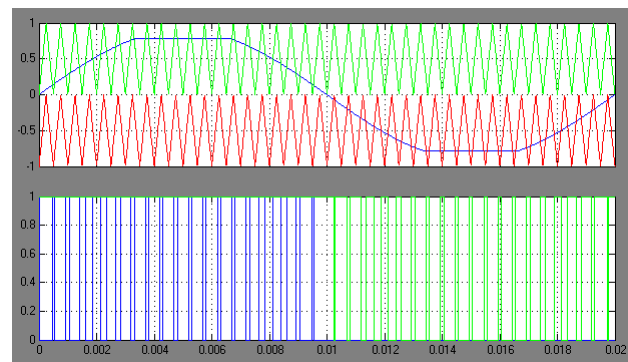


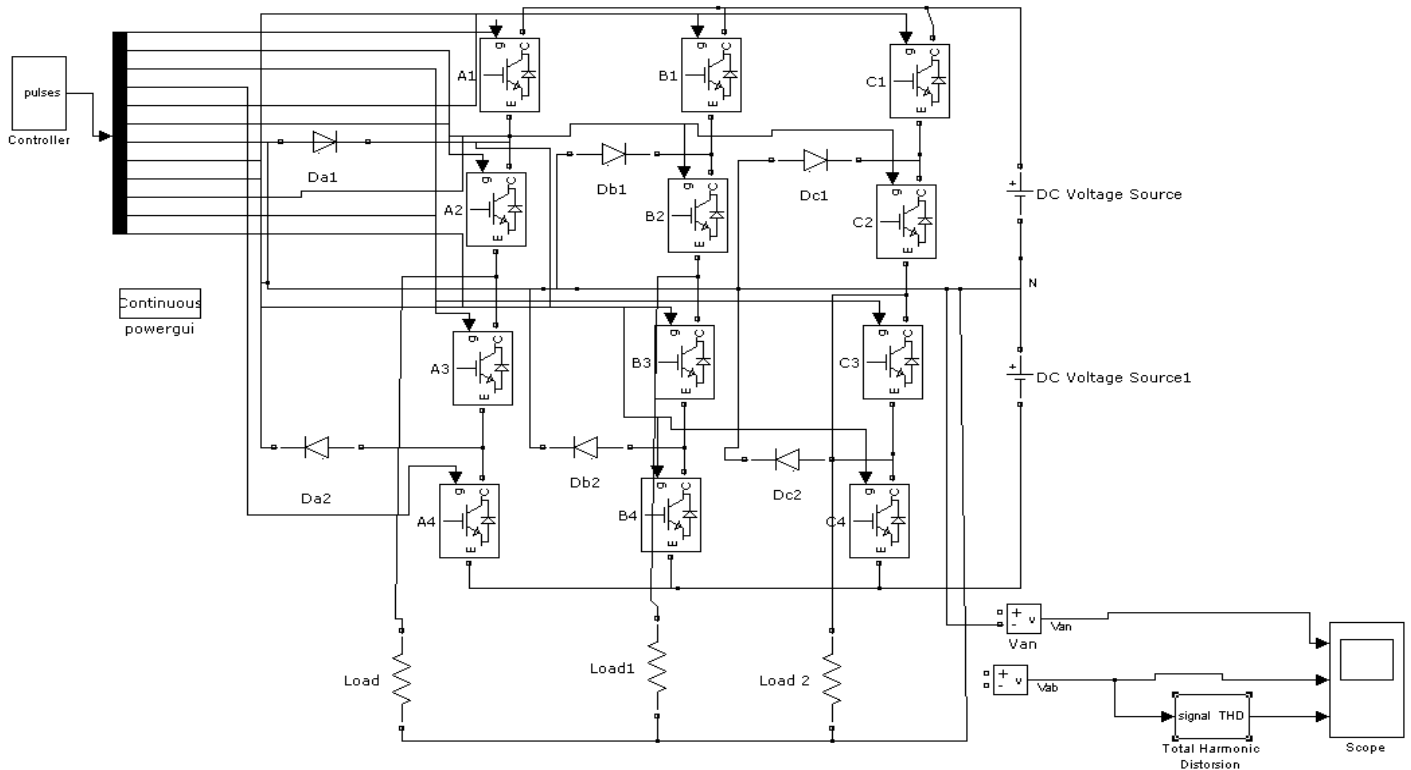
Fig 5: Sixty degrees PWM technique

## 2. VARIATION OF THD WITH MODULATION INDEX IN SINUSOIDAL PWM METHOD

From Figure 3, modulation index can be defined as

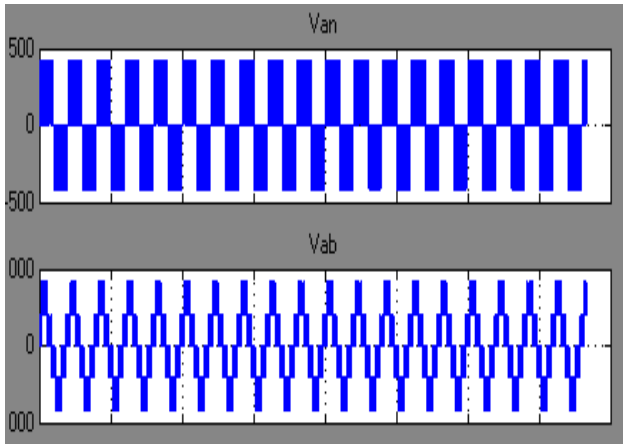
$$m = \frac{\text{PeakvalueofSinewave}}{\text{PeakvalueofTriangularwave}}$$

The simulation model of control circuit is as shown in Figure 6.



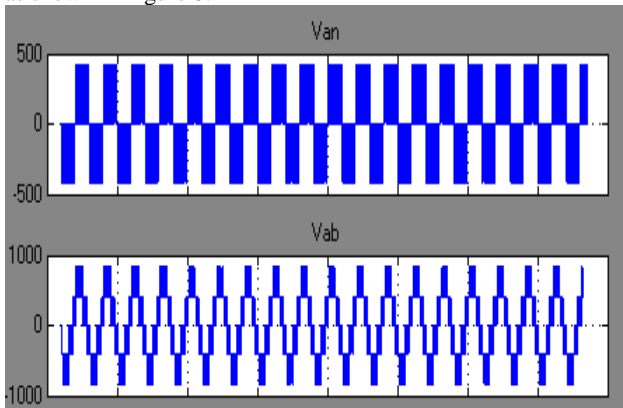
**Figure 6: Control Circuit**

Here, a three level diode clamped inverter is controlled by sinusoidal PWM. Pulses block generates pulses for all the switching devices. DC side has two voltage sources, each of 400V. Total Harmonic Distortion block given in the circuit measures the THD for various values of modulation index, m. Modulation index is the ratio of magnitude of reference wave to magnitude of high frequency carrier wave. Output phase to neutral and phase to phase voltages for m=0.7 are as shown in Figure 7:



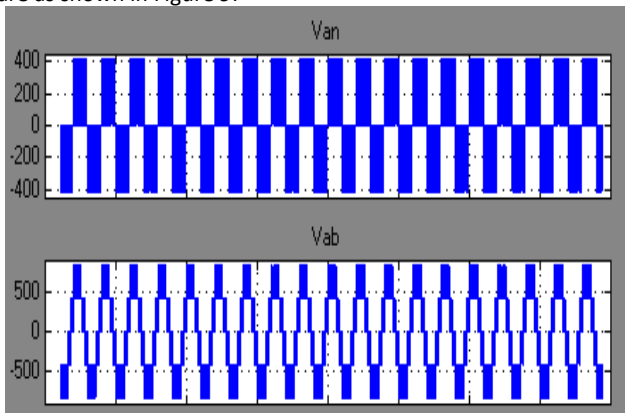
**Fig 7 : Output waveforms for m=0.7**

Output phase to neutral and phase to phase voltages for m=0.8 are as shown in Figure 8:



**Fig 8 : Output waveforms for m=0.8**

Output phase to neutral and phase to phase voltages for m=0.9 are as shown in Figure 9:



**Fig 9: Output waveforms for m=0.9**

Variation of THD with modulation index is as given in Table 2. It is clear from Table 2 that as modulation index increases, the Total Harmonic Distortion decreases.

Also from Figures 7, 8, 9, as modulation index increases, the width of middle notch in  $V_{ab}$  increases.

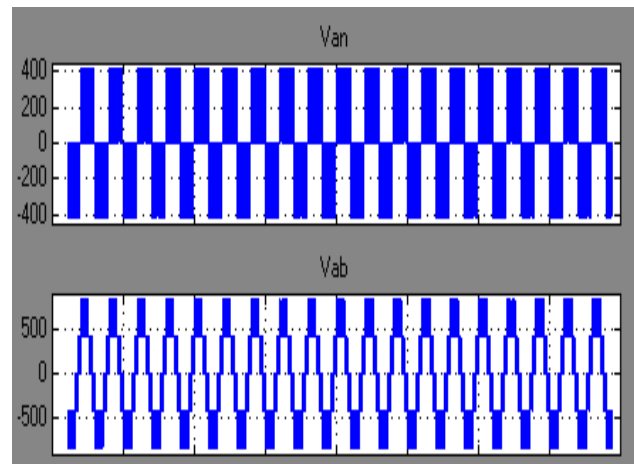
**Table 2 . Variation of Total Harmonic Distortion with m**

Sno	m	THD
1	0.7	0.44
2	0.75	0.43
3	0.8	0.42
4	0.85	0.41
5	0.9	0.39
6	0.95	0.37

### 3. VARIATION OF MODULATION INDEX WITH CONTROL STRATEGY

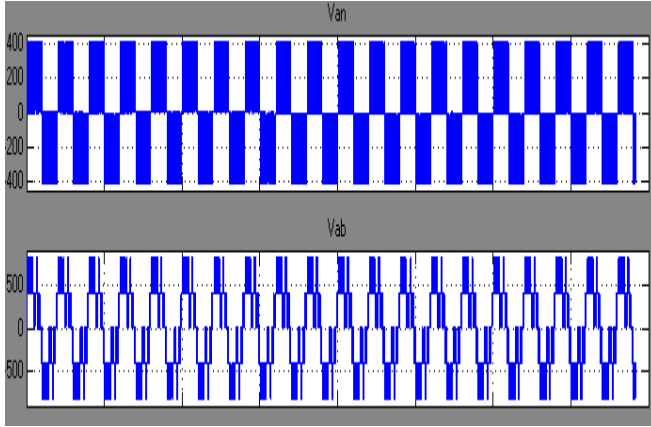
The control circuit shown in Figure 6 is controlled with Sinusoidal PWM, Third harmonic injection PWM and Sixty degree PWM methods and the following results were obtained.

Output phase to neutral and phase to phase voltages of Sinusoidal PWM controlled Diode clamped multilevel inverter is as shown in Figure 10.



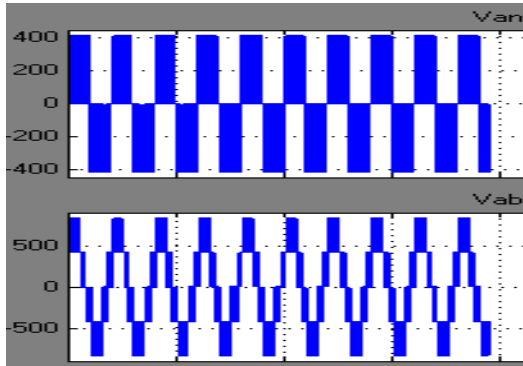
**Fig 10. Output waveforms for Sinusoidal PWM controlled multilevel inverter**

Output phase to neutral and phase to phase voltages of Third harmonic injection PWM controlled Diode clamped multilevel inverter is as shown in Figure 11.



**Fig 11 : Output waveforms for Third harmonic injection PWM controlled multilevel inverter**

Output voltages and THD of Sixty degree PWM controlled Diode clamped multilevel inverter is as shown in Figure 12.



**Fig 12. Output waveforms for Sixty degree PWM controlled multilevel inverter**

THD values for these three control techniques is as given in Table 3.

**Table 3. Variation of THD with control technique**

Sno	Control Strategy	THD
1	Sinusoidal PWM	0.39
2	Sixty degree PWM	0.48
3	Third harmonic injection PWM	0.57

#### 4. CONCLUSION

A Diode Clamped Multilevel inverter is controlled by Sinusoidal PWM, Third harmonic injection PWM and Sixty degrees PWM methods. Variation of THD with respect to control strategy is as

given in Table3. Considering a resistive load, Sinusoidal PWM method provides lowest THD. Variation of THD with respect to modulation index is as shown in Table 2. As modulation index increases, THD decreases.

#### 5. ACKNOWLEDGMENTS

Our thanks to the experts who have contributed towards development of the template.

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