Design and Simulation of SR, D and T Flip- Flops modeled with Single Electron Devices

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ABSTRACT

The inspiring aspect of SET technology is that it offers control over the movement of one individual electron in the SEC (single electron circuits). In this paper we present SET (single electron tunneling) gate based implementations of SR flip-flop, D flip-flop and T-flip-flops. The whole design and simulation is made using a Monte- Carlo based tool. We propose gate based design of these SECs and verify simulation results using Monte Carlo Simulator (SIMON 2.0). The operation of the basic flip flops is successfully demonstrated through SIMON circuit simulation.

Keywords: Coulomb Blockade, Single Electron Transistor SET, tunneling, Quantum Dot, Tunneling Rate, SR flip flop, D flip flop and T flip flop, SIMON

1. INTRODUCTION

Single-electron technology have attracted much attention as an area for achieving high functional density, low power nano-electronic devices and extremely fast switching devices in principle. The operation of Single Electron Device is based on the Coulomb blockade which appears in a nanostructure and is observed and studied at a very low supply voltage by Gorter [1]. The main component of the SET circuits is the tunnel junction through which individual electrons can move in a controlled manner [3]. SET technology hence has a tremendous potential for the development of future miniature circuits. So far, works on gate based novel half-adder [2], set logic gate families [4], single-electron full-adder [5], digital-quantizers [6], NAND gate [7], Programmable Logic Arrays [8] etc. have been proposed. In section II, some basic and applicative literature SET technology are reviewed. Section III presents our proposed design (inclusive of the detailed schematic diagrams and parameters) and simulation results using Monte Carlo [9] Simulator (SIMON 2.0[10]). We conclude in Section IV by providing some future scope of work followed by providing the used references in Sec V.

2. SINGLE ELECTRON TRANSISTOR DEVELOPMENT

SETs are devices in which the charge transport is discrete in nature unlike MOS devices. Fig 1. shows the basic build up of a SET where a controlled flow of current becomes realizable. [11] [12] [13] [14]. A SET is made from two tunnel junctions that share a common electrode as shown in Fig1. A tunnel junction consists of two pieces of metal supported by a very thin (about 1 nm) insulator. The only way for electrons is one of the metal electrodes to travel to the other electrode to tunnel through the insulator.

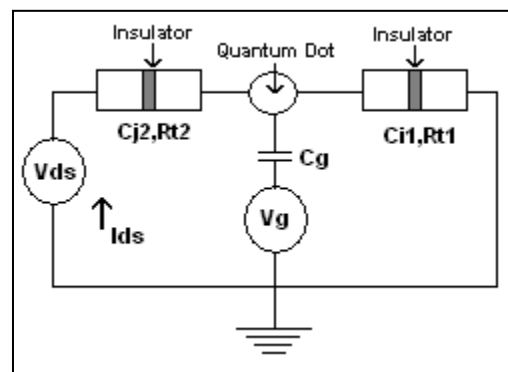Since tunneling is a discrete process, the electric charge flows through the tunnel junction in multiples of e.

Fig1. Building blocks of SET

Now if the bias voltage V is kept below the Coulomb gap voltage and if the gate voltage is increased, the energy of the initial system (with no electrons on the island) gradually increases, while the energy of the system with one excess electron on the island gradually decreases. The fundamental principle of single-electronics is that one needs coulomb energy E_c to charge an island with an electron. The energy is given by:

$$Ec = \frac{e^2}{2c_i} > kT \qquad (1)$$

Where e is the elementary charge and C_i is the capacitance of the island. Through the tunnel junctions electron tunnels independently from island to island. To make sure that the electron states are localized on the islands, all tunnel resistances must be larger than the fundamental resistance R_q:

$$R > R_q = \frac{h}{e^2} = 25.813 \,\Omega \qquad (2)$$

At the gate voltage corresponding to the point of maximum slope on the Coulomb staircase, both of the charge of electrons.[1] The QD (quantum dot) is connected to the source and drain electrodes through tunnel barriers. The potential in the dot can be controlled by the gate electrode which is capacitive coupled to the QD [15]. The current through the dot can be periodically modulated by the gate voltage (Coulomb oscillations). When the current is zero (Coulomb blockade [1]), the number of electrons is fixed.

The essentials of proper operation of a SET devices becomes;(a) the tunnel junction resistances (drain resistance, R_D

and source resistance, R_S) to be greater than the quantum resistance (25.8 kΩ) [16] to confine the electrons in the QD, (b) the charging energy of the QD capacitance to be larger than the available thermal energy to avoid electron tunneling due to the thermal emission, and the total capacitance of QD is equal to the sum of all device capacitances, i.e. $C_T = C_G + C_D + C_S$.

To simulate the tunneling of electrons from island to island in a single-electron circuit one has to determine the rates of all the possible tunnel events. When a tunnel event occurs the circuit's free energy changes. This free energy change will determine the tunnel rate of a possible tunnel event. What is meant by the free energy F of a single-electron circuit is the difference between and the electrostatic energy U stored in its capacitance and the work done by the voltage sources of the circuit W.

$$\mathbf{F} = \mathbf{U} - \mathbf{W} \qquad (3)$$

The tunneling rate for a particular tunnel event is given by

$$\Gamma = \frac{\Delta F}{e^2 R_T \ (1 - e^{-\frac{\Delta F}{kT}})} \qquad (4)$$

Where ΔF is the change in the free energy caused by this particular tunnel event, R_T is the tunnel resistance of the tunnel junction through which the electron is transported, KT is the thermal energy (k is the Boltzmann's constant, and T is the temperature). When the tunnel rates for all the possible tunnel events are known, the event actually occurring is determined by using the Monte Carlo method, combined with an exponential distribution of tunnel events . The time duration of a particular tunnel event is given by:

$$\Delta t = -\frac{\ln(r)}{\Gamma} \qquad (5)$$

Where r is an evenly distributed random number in the interval [0,1]. Among all the possible tunnel events, the event with the shortest time duration takes place.

3. GATE BASED FLIP-FLOPS

A. SR FLIP-FLOP (SR-FF)
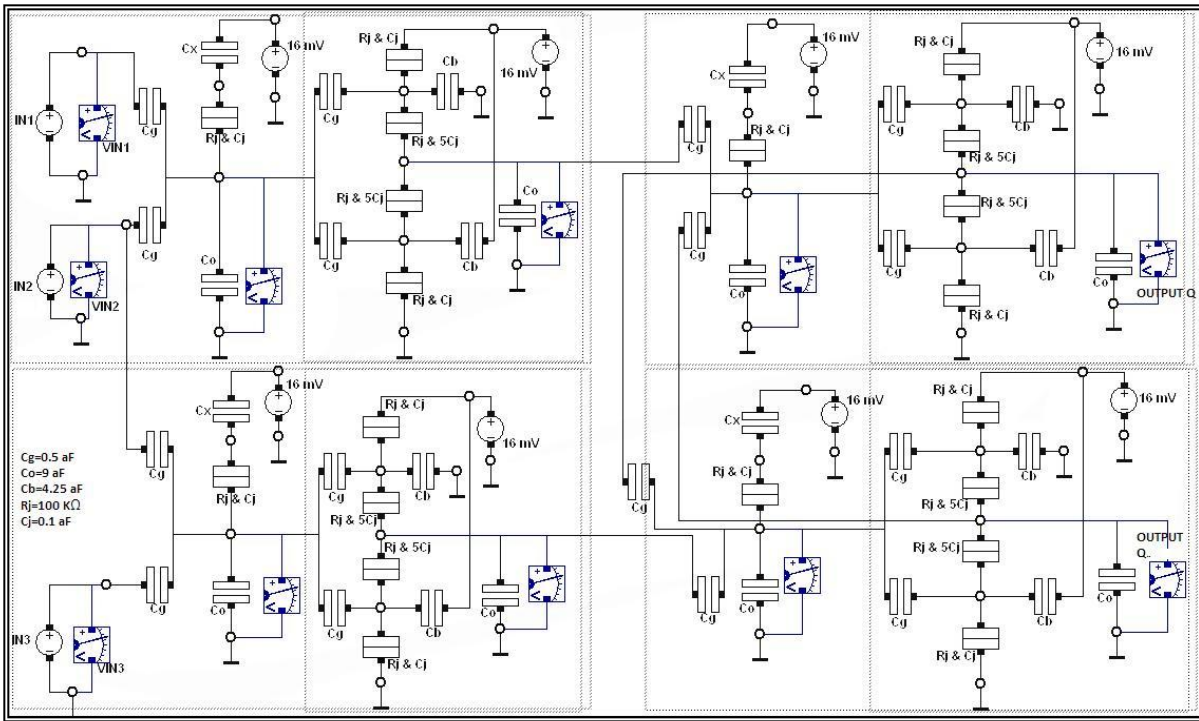
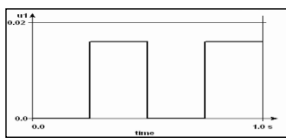**Fig.2. Circuit Schematic of gate based SR-FF**
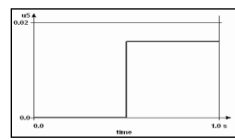

Fig.2 (a) S-Excitation at IN_1

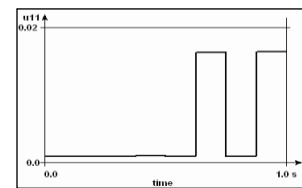**Fig. 2(b) R-Excitation at IN_3**

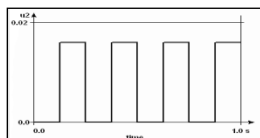
Fig 2(e) Complimentary output Q' for SR-FF

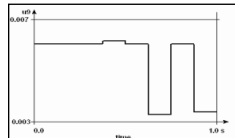**Fig 2(c) Clock at IN_2 for SRFF**

Fig 2(d) Output Q for SRFF

The above circuit is based on the basic gate based SRFF. In the circuit shown in Fig.2, V_{IN}=16mV (logic'1'), and V_{IN}=0V (logic '0'). Gate capacitance (C_g) is 0.5aF; tunnel resistance (R_j) is 100KΩ; back capacitance (C_b) is 4.25 aF; and load capacitance (C_o) is 9aF.

IN$_1$ and IN$_3$ are the S and R excitations respectively and IN$_2$ is the clock. Here, 2 AND gates and 2 NOR gate have been used to simulate the SR Flip-Flop. The inner dotted blocks show the respective gates. There is a sudden bulge in the output at the 2nd Clock Pulse. This happens because of the free energy discharge from the circuit. Thus, the free energy of the circuit should always be kept least possible, since it may result in undesirable outputs.
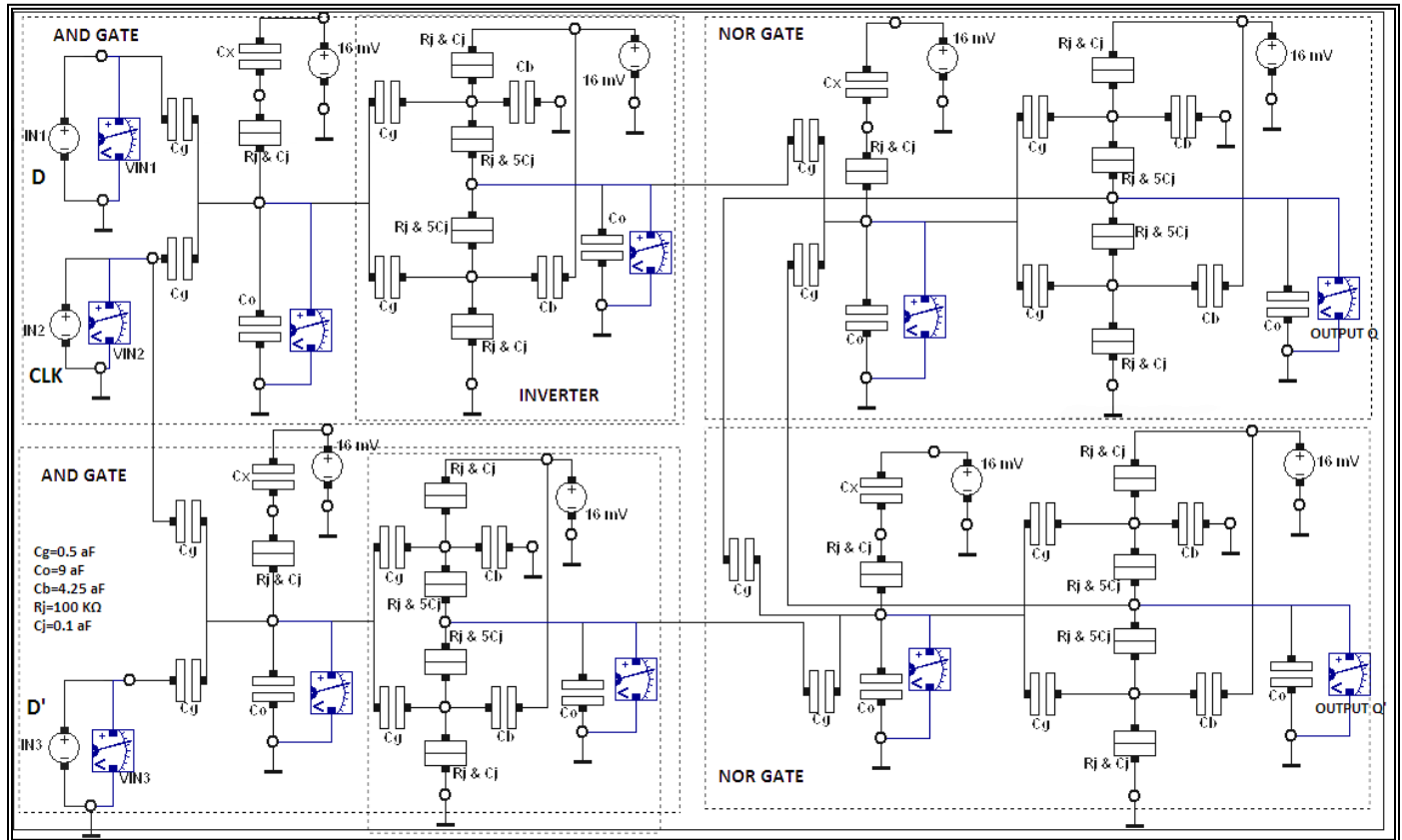
B.   D FLIP FLOP

Fig.3. Circuit Schematic of gate based D-FF
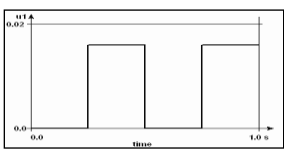
Fig 3(a) Input excitation D at IN$_1$
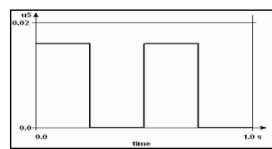
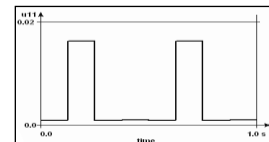**Fig 3(b) Input excitation D' at IN$_3$**

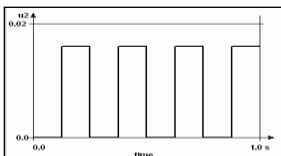**Fig 3(e) Complimentary output Q' for DFF**

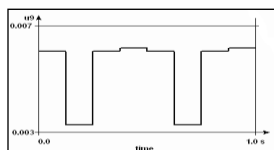
Fig 3 (c) Clock at IN$_2$ for D-FF

Fig 3(d) Output Q for DFF

The bulge at the output after the second clock pulse also happens because of the reasons specified before. Here, 1 Inverter, 2 NAND gates and 2 OR gates have been used to simulate the D-FF. The internal parameters of the gates remain the same as for SRFF.

C. JK Flip-Flop (JK-FF)

In a similar way a gate based JKFF is constructed as shown in Fig 4. Here IN$_1$ is the K excitation (Fig. 4(b)), IN$_3$ is the J excitation (Fig. 4(a))and IN$_2$ is the clock (Fig. 4(c)).
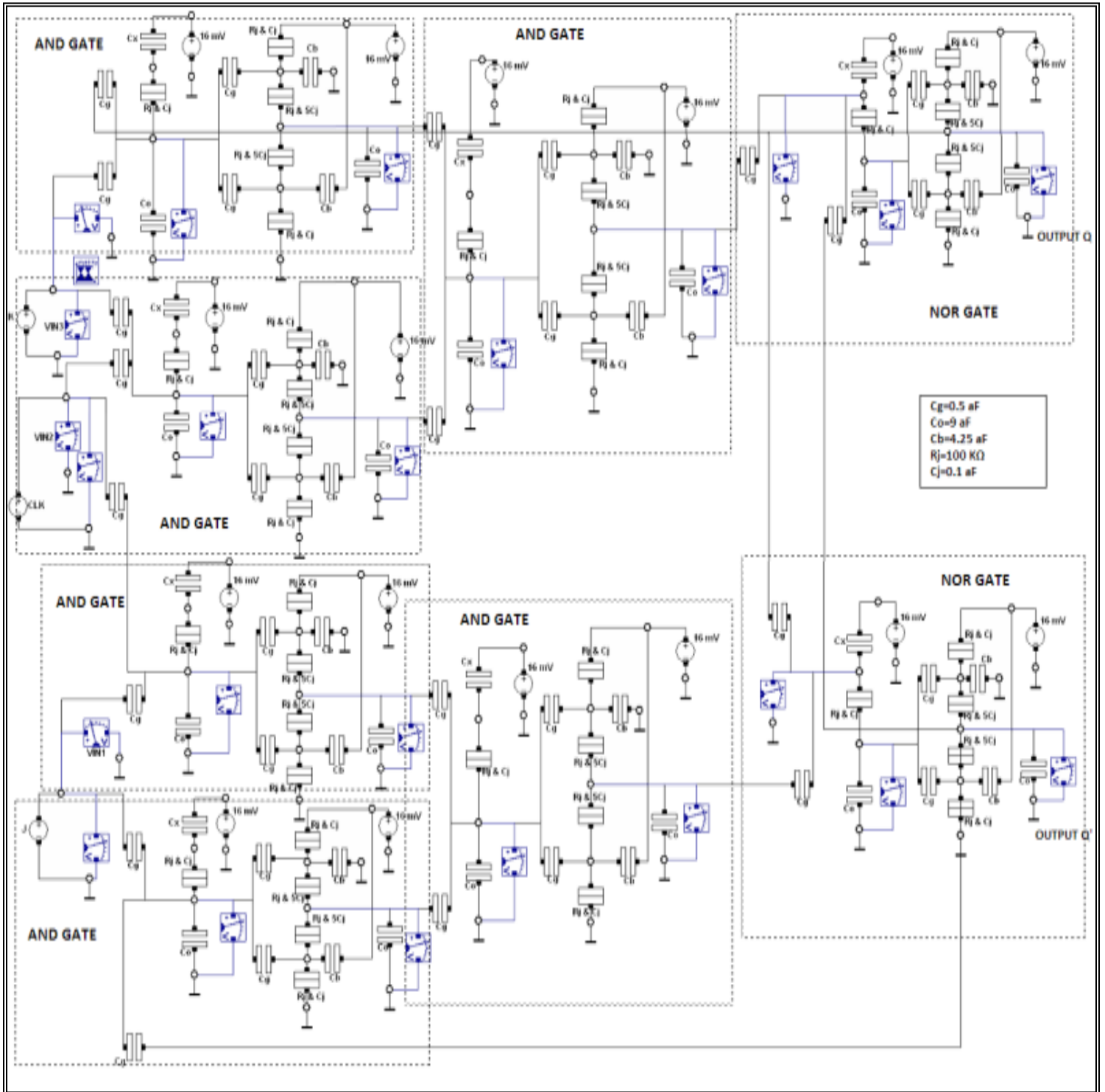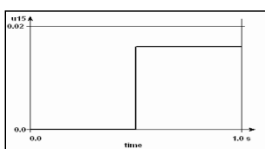
Fig 4. Circuit Schematic of gate based JK-FF

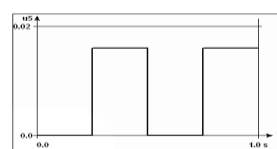
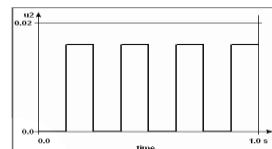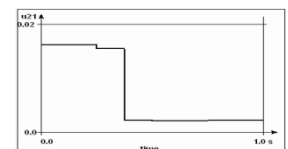Fig 4(a) J excitation for JKFF Fig 4(b) K excitation for JKFF Fig 4(c) Clock for JKFF Fig 4(d) Output Q for JKFF
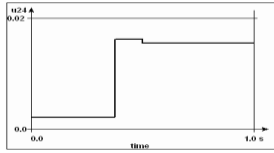
Fig 4(d) Complimentary Output Q' for JKFF

To construct a JKFF, two 3-Input AND gates and two 2-Input NOR gates have been used. A 3-Input AND gate is realised using two 2-Input AND gates because of which the circuit becomes large.
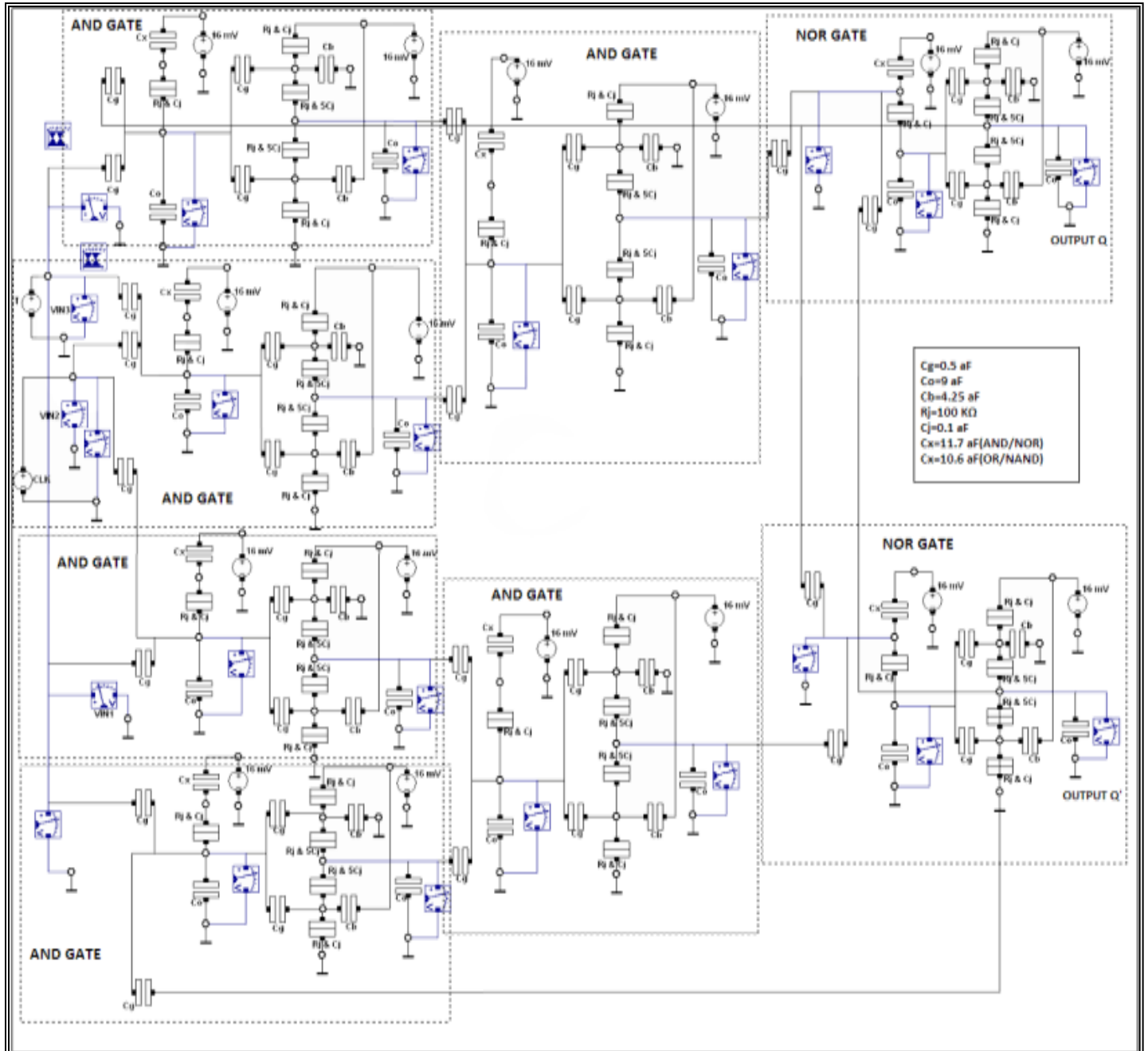

Fig 5. Circuit Schematic of gate based T-FF.

D.   T-Flip-Flop (TFF)

T-FF (Fig 5) is also constructed in a way similar to JK-FF wherein the T excitation (Fig 5(a)) is obtained by shorting the J and K

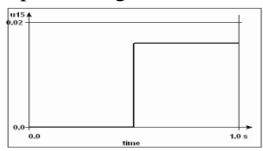excitations of JKFF. Here too, two 3-Input AND gates and two 2-Input NOR gates have been used as JKFF.

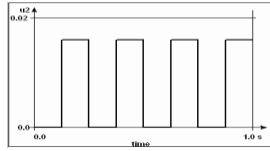**Fig5(a) T excitation as seen at VIN_3**
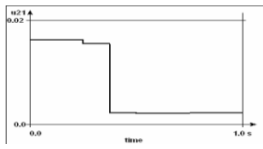

Fig 5(b) Clock as seen at IN_2

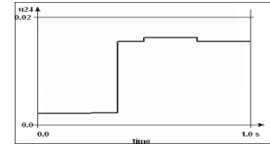**Fig 5(c) Output Q for T-FF**

Fig 5(d) Complimentary output Q' for TFF

4 .CONCLUSION AND FUTURE PROSPECTS

The design and simulation of a single-electron flip-flops has been presented in in this paper, done using a Monte-Carlo based tool. A step wise procedure was followed, designing first the basic fundamental gates, exploring its operational characteristics and verifying the behavior of the flip-flops. The proposed work can be extended to make larger circuits like counters and shift registers. Further more the Monte Carlo method provides accuracy but lacks time efficiency required for large scale simulation. Adaptive simulation has been used which when compared to the non-adaptive approach, the simulation time were reduced by upto 40 times while the average error was 3.3% [17]. Since SETs are known to drive very less current and CMOS are known to have been operated at realistic temperatures, **SET-CMOS** hybrid circuits can be simulated using **SMARTSPICE** simulators that can provide simulation results with more accuracy.

5. ACKNOWLEDGEMENT

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