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A Novel and Efficient Approach for RC Delay Evaluation of On-chip VLSI Interconnect under Current Mode Signaling Technique

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ABSTRACT
Current-mode signaling significantly increases the bandwidth of on-chip interconnects compared to voltage mode signaling and reduces the overall propagation delay. A delay formula for current mode is necessary for estimation of delay and bandwidth for VLSI systems. In this paper, closed-form expression of delay model based on the effective lumped element resistance and capacitance approximation of distributed RC lines are presented. A new closed-form solution of delay under step input excitation is developed. The usefulness of this solution is that both resistive and capacitive load termination is accurately modeled for use in current mode signaling**.** Comparison of simulation results with other established models justifies the accuracy of our approach.

Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design Aids – Simulation;

General Terms
Algorithms, Design, Theory

Keywords
Current mode signaling, On-chip Interconnect, Moment matching, MNA Analysis, Delay Calculation.

1. INTRODUCTION
The continuous miniaturization of integrated circuits has opened the path towards System-on-Chip realizations. Process shrinking into the nanometer regime improves transistor performance while the delay of global interconnects, connecting circuit blocks separated by a long distance, significantly increases. Signaling across long global on-chip interconnects is rapidly becoming a performance limiter due to reverse interconnect scaling trends. As an alternative to traditional voltage mode (VM) signaling, signaling techniques based on current-mode (CM) signaling allows for high-speed data transmission due to the improvement in interconnection bandwidth. Various techniques based on simulations and/or analytical closed-form formulations have been proposed to model delay in interconnects [1-3] using the VM signaling concept .Current mode signal transporting techniques may provide an attractive solution to some of the challenges caused by aggressive Interconnect scaling.

A useful closed-form delay analysis of current mode signaling for RC interconnects was presented in [4]. However, the analysis assumes the output response is a linear-ramp signal and does not include transient effects due to a step or fast edge rates inputs. In this work, we present an analytical model based on the closed-form formulation of the effective resistance and capacitance of a driven distributed RC line with arbitrary termination. [10] is based on this model and by satisfying the boundary conditions, a new closed-form single exponent approximation of interconnection delay under step input excitation is derived for arbitrary load terminations. It is shown that the accuracy of this work is the same as Sakurai's voltage mode formulation [5], extended herein to accommodate current-mode type circuits.

The closed-form delay expression presented in this paper provides fast delay estimation at only a first order complexity. The model is derived using recurring MNA (Modified Nodal Analysis) to obtain the equivalent resistance and capacitance.

2. RC DELAY FORMULATION FOR CURRENT MODE SIGNALLING

2.1 Basic Theory
Long global interconnects can be modeled by distributed RC transmission lines as long as the overall line resistance dominates the response (i.e. $R>>jwL$). From a signaling point of view, both voltage and current mode drivers can be approximated by a voltage source and a linear resistance. Current-mode receivers, on the other hand, provide a low impedance node at the receiver whereas voltage-mode receivers present a high impedance capacitive termination. R_L and C_L are determined from the receiver circuit topologies

A generalized model for a driven distributed RC line is shown in Figure 1(a). The diver is modeled as a voltage source with output resistance R_S. For the sake of generality the output of the line is terminated with a resistor R_L, and load capacitance C_L. For voltage-mode signaling, the termination resistance R_L is infinite and the output voltage is seen across C_L. In current mode signaling, the terminating resistance R_L is finite.

2.2 MNA for Closed form Derivation

Moment-Matching Methods [6-7] can be used to derive a first-order network with effective lumped element parameters for voltage and current mode signaling. It is well understood that a lumped, linear, time-invariant circuit such as that of a generalized distributed RC line shown in Figure 1, can be conveniently expressed in terms of state equations by using the modified nodal admittance matrix (MNA) representation [8][9]. The generalized

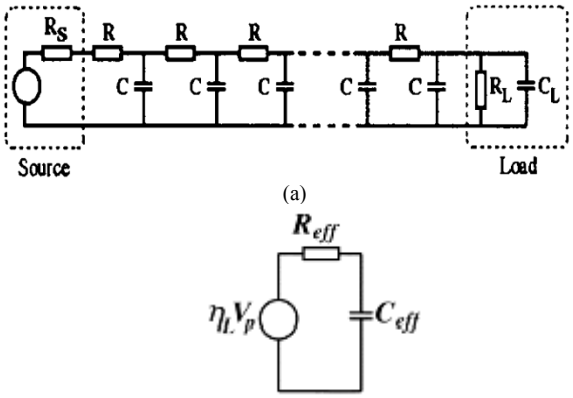

Figure 1. (a) Generalized distributed RC model (b) Approximate effective lumped element model

output equation can be expressed in the Laplace domain as:

$$[G + sC]\cdot[X(s)] = b(s) \quad (1)$$

Where G and C are the nodal conductance and capacitance matrices, respectively as shown in Figure 1. X is vector of node voltages and $b(s)$ is the input source excitation.

$$[G] = \begin{bmatrix} G_E+G_u & -G_u & 0 & \dots & \dots & 0 \\ -G_u & 2G_u & -G_u & 0 & \dots & 0 \\ 0 & -G_u & 2G_u & -G_u & 0 & \dots \\ \dots & \dots & \dots & \dots & \dots & \dots \\ \dots & 0 & -G_u & 2G_u & -G_u & 0 \\ \dots & \dots & 0 & -G_u & 2G_u & -G_u \\ 0 & \dots & 0 & 0 & -G_u & G_L+G_u \end{bmatrix} \quad (2)$$

G_u is the segment conductance of the distributed transmission line and G_L is the load conductance. $G_E = l/(R_s+R_u)$; where R_s is the source resistance.

The vector of node voltages of X is expanded into a Taylor series to obtain the moments M in (2), where the subscript of Mq indicates the order of the moments. By equating the moments of same order on both sides of (2), a final recursive relationship is obtained to derive the moment as shown in (3).

$$[G + sC]\cdot[M_0 + M_1 s + M_2 s^2 + \dots] = b(s) \quad (3)$$

So, $[G]\cdot M_0 = b$

And $[G]\cdot M_q = [C]\cdot M_{q-1} \quad \forall q > 0$ (4)

Where M_q represents the moment vector of the transfer function $H(s)$ of Figure 1(a). A general closed-form expression for the q^{th} moment and the k^{th} node voltage of $X(s)$ is given by:

$$m_{q+1}^k = \sum_{i=1}^{N} -G_{inv}(k,i)\cdot C(i)\cdot m_q^i \quad (5)$$

Where N is the number of distributed segments and G_{inv}, is the inverse matrix (G^{-1}) which can be expressed as (A):

$$G_{inv}(k,i) = \begin{cases} \dfrac{[G_u + (N-k)G_L]\cdot[G_u + (i-1)G_E]}{G_u[G_u G_E + (N-1)G_L G_E + G_L G_u]} & \in i \le k \\ \dfrac{[G_u + (N-i)G_L]\cdot[G_u + (k-1)G_E]}{G_u[G_u G_E + (N-1)G_L G_E + G_L G_u]} & \in i > k \end{cases} \quad (A)$$

From the 0^{th} and 1^{st} moments, the distributed network can be approximated to the 1st order transfer function as shown in (6), where p is the dominant pole that determines the delay of the line.

$$\hat{H}(s) = \frac{\hat{k}}{s+\hat{p}} = \frac{m_0^N\left(-\frac{m_0^N}{m_1^N}\right)}{s+\left(-\frac{m_0^N}{m_1^N}\right)} \quad (6)$$

2.3 Effective Resistance and Capacitance

Since the pole of $\hat{H}(s)$ is 1/ (R_{eff} C_{eff}), the effective resistance and capacitance is derived from (5), which can be written in closed-form as:

$$R_{eff} = \alpha\frac{R_t}{\sqrt{2R_L}}\left(\frac{N-1}{N}\right)\left[R_S + R_L + \frac{R_t}{3}\left(\frac{N+1}{N}\right)\right] + 2\frac{\alpha}{\sqrt{2}}\left[\frac{NR_S + R_t}{N}\right] \quad (7)$$

$$C_{eff} = \frac{c_t}{\sqrt{2}} + \alpha C_L\left[\frac{R_S + R_t}{R_{eff}}\right] \quad (8)$$

$$\alpha = \frac{R_L}{R_L + R_S + R_t} \quad (9)$$

R_s and R_L are the source and load resistance respectively. R_t and C_t are the total resistance and capacitance calculated from the

unit length components R and *C*, and total interconnect length *l; N* is the number of distributed segments.

Thus the distributed transmission line can be effectively modeled by the lumped element resistance and capacitance given in (7-8). The generalized effective lumped element model is shown in Figure 1(b). For current mode signals the source voltage (V_s) is scaled by α. The usefulness of this model is that an equivalent lumped element model can predict the step response of an interconnect line for both current and voltage model.

3. DELAY ANALYSIS UNDER STEP INPUT EXCITATION

In Figure 2, the distributed line with 1000 segments and lumped element model with effective resistance and capacitance is shown. Since we considered single dominant pole, the effective model voltage response in (6-8) will cross over the distributed output response at approximately 62% of the normalized output voltage. An improved analytical approximation of the delay can be obtained by satisfying the boundary conditions at $v_{0.62}$ and v_i, with a single exponent, as shown in Figure 2.

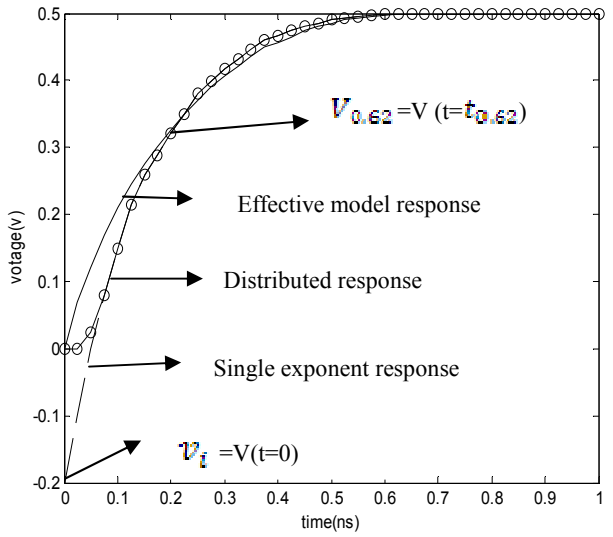

Figure 2. Single exponential Function Approximation for the step response of a distributed line

The new normalized expression can be given by:

$$V(t) = 1 - (1 + v_i)e^{-\frac{t}{RC}} \qquad (10)$$

Where RC is the time constant of the new single exponent approximation function. By forcing the boundary condition at *v (t=t0.62)*, the following relationship is obtained:

$$t_v = \frac{\ln\left[\frac{1+v_i}{1-V}\right]}{1 - \frac{\ln(1+v_i)}{\ln(0.38)}} R_{eff} C_{eff} \qquad (11)$$

An optimum value of vi was found iteratively which is approximated by:

$$v_i = v(t=0) = 0.5\alpha \frac{R_t}{R_L} + 0.2 \qquad (12)$$

For an input step excitation, the final expression for current mode and voltage mode signal can be derived by using (7-8) (11) and (12).

$$\frac{t_v}{R_t C_t} = \frac{\ln\left(\frac{1.2 + 0.5\left(\frac{\alpha}{R_{LT}}\right)}{1-V}\right)}{1 + 1.0335 \ln\left(1.2 + 0.5\left(\frac{\alpha}{R_{LT}}\right)\right)} \cdot R_E \qquad (13)$$

Where

$$R_E = \left[\frac{\alpha}{2}\left(R_{SL} + 1 + \frac{1}{3R_{LT}}\right) + \alpha\left[\frac{NR_{ST}+1}{N}\right] + \alpha C_{LT}(R_{ST}+1)\right] \qquad (14)$$

Where RLT $=R_L/R_t$, $R_{ST}= R_S /R_L$, $C_{LT}=C_L /C_t$, RSL$=R_S /R_L$ the term R_E depicts the contribution of the normalized source and load terminations (i.e., R_{ST}, R_{LT} and C_{LT}), exhibiting great similarity to the equations derived by Sakurai [5]. The analytical formula of voltage mode signal matches well with the Sakurai model which is determined to have an error less than 3.5% for a large range of parameters'. This accuracy is also maintained for current mode signals across a wide range of values.

4. RESULTS OF THE DELAY RESPONSE AND THE EQUATION

We computed the delay for current mode signaling using HSPICE simulator keeping R_L =500Ω. We compare our delay with [10] and distributed delay response with 1000 segments. We call these delays as BshD and DtdD, respectively. For V=0.8 Volt and R_L=500 Ω the results of our model are almost equal to the distributed response and BshD. The comparison of our delay (RD) with BshD and DtdD is shown in Table 1. From Table 1 we find that our model provides the accurate delay estimation compared to other approaches and results an average error of 4.7% for large range of parameters. Where '*V*' represents the normalized threshold voltage and RC represents the product of the distributed unit segment. We can easily extend our result to voltage mode (By putting $R_L = \infty$ and $R_S = 0$). If we do so, we will get the similar expression as that of [5].

Table1. Delay comparison with Distributed delay and [10]

V=0.9volt ,R_L=500 Ω			
	Delay (ns)		
RC(ns)	Bas D	Dtd D	R D
1	0.90	0.89	0.897
2	1.41	1.405	1.408
3	1.90	1.86	1.88
4	2.35	2.29	2.33
5	2.73	2.68	2.72
V=0.8volt ,R_L=500 Ω			
	Delay (ns)		
RC(ns)	Bas D	Dtd D	R D
1	0.67	0.667	0.67
2	1.121	1.12	1.121
3	1.42	1.41	1.425
4	1.67	1.66	1.67
5	2.23	2.20	2.22
V=0.7volt ,R_L=500 Ω			
	Delay (ns)		
RC(ns)	Bas D	Dtd D	R D
1	0.52	0.52	0.52
2	0.867	0.87	0.868
3	1.11	1.12	1.115
4	1.40	1.41	1.406
5	1.68	1.69	1.68

5. CONCLUSION

A closed-form 50% delay formula for the current mode interconnects with a step excitation is derived. Compared to HSPICE simulation, the current mode RC model achieves an average error of 4.7% over a wide range of typical parameters. The usefulness of this model is that an equivalent lumped element model can predict the step response of an interconnect line for both current and voltage mode signaling. The derived expression along with this analysis can serve as a convenient tool for delay estimation without much computation during design.

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