A 100KHz – 20MHz source follower continuous time filter for SDR applications

S.Ramasamy, S.Kumaravel and Dr.B.Venkataramani

ABSTRACT

The source follower based filters are proposed in the literature for wireless LAN applications and are preferred as they dissipate lower power compared to the filters using other architectures. To comply with multitude standards, filters with bandwidth programmable from 100KHz – 20MHz are required. In this paper, a second order, composite source follower based filter is made to work in weak inversion in order to achieve wide tuning range and to minimize power consumption. The centre frequency of this filter is varied using current steering DAC. The proposed filter is designed and implemented on TSMC-0.18µm CMOS process with 1.2V supply. The simulation results demonstrate the tunability of the centre frequency from 100KHz to 20MHz which meets the requirements of zero IF receivers for SDR applications. The third order input intercept point (IIP3) is found to be 15 dBVp for an input signal of 200mVp. The power dissipated by the filter is 1µW and 20µW at 100 KHz and 20 MHz respectively. The proposed filter consumes 14 times less power than that proposed in the literature at the cost of 1.5 times increase in the noise. A 55µVrms noise gives a dynamic range of 66dB.

Keywords

analog baseband filter, continuous-time filter, Software Defined Radio, subthreshold, reconfigurable filter, source follower, current steering DAC.

1. INTRODUCTION

The growing popularity and importance of mobile communication, and the evolution of different standards for voice and data are pushing the research towards the implementation of fully integrated multi standard transceivers [1]- [6]. Such transceivers should switch seamlessly among different standards in order to achieve the so-called "global roaming" for both voice and data applications. GSM and WCDMA (UMTS) are the dominant standards for voice and mixed voice/data mobile services, while WLANs based on the IEEE 802.11a/b/g protocols are the most important standards for high data rate wireless internet access. Finally, bluetooth protocol enables wireless connectivity for various appliances at low data rates over a short distance. This multitude of standards requires multimode terminals to be capable of adjusting their configuration and reception mode depending on the standard and quality of service requirements. In addition to meeting the traditional performance metrics such as power, area and price, a single handset should now comply with this multitude of standards. A software defined radio (SDR) proves to be a promising technology for this demand. In these systems, analog baseband filter plays a key role as it provides channel selection and anti-aliasing. For SDR applications [1], zero IF receivers are commonly used. In this paper, a low-pass filter capable of being tuned over a wide range of frequencies suitable for zero-IF receiver is proposed.

Continuous time filters are quite suited for applications with moderate speed and low power requirements. Traditionally, continuous time CMOS filters with G_m-C architecture have been designed with MOS transistors operating in strong inversion region when bandwidth of interest is of the order of several tens of MHz. A number of architectures have been proposed in the literature for implementing the transconductor. Analog baseband filters for UMTS/WLAN applications have been proposed using active R-C cells in [4] and Active G_m-RC in [5]. The latter scheme requires less area as it shares the capacitor for various applications. Continuous time filter using switchable operational amplifier and capacitor arrays is proposed in [6] to achieve flexible trade off between power and bandwidth. A G_m–C Low-pass Filter for zero-IF Mobile Applications with a tuning range of 100 KHz to 2.11MHz is achieved in [7] using Si-Ge process. Push-pull inverters are proposed in [8] for realizing the transconductor. This does not have any internal node and results in large bandwidth. However, for realizing programmable filters, this scheme requires the power supply voltage to be varied. This is not suitable for low voltage applications and it results in poor power supply rejection ratio (PSRR) [8]. To solve this problem, floating battery implementation is proposed in [9]. But this scheme requires a large bias resistor, which introduces an additional pole in the region of interest.

Crombez et al [10] uses Nauta's [8] architecture with novel, but complex switching scheme to satisfy noise and linearity levels for reconfigurability with provision for independent transconductance and capacitance tuning. However, it uses complex switching mechanism and its power consumption is high. The source follower filter for WLAN applications reported in [11] consumes less power but does not have programmable bandwidth feature. In this paper, a second order, composite source follower based filter is made to work in weak inversion in order to achieve wide tuning range and to minimize power consumption.

This paper is organized as follows. Section 2 describes source follower based second order low pass filter operating in weak inversion region. Section 3 presents the structure of the DAC system for bandwidth programmability. The simulation results are given in Section 4 followed by the conclusions in Section 5.

2. THE PROPOSED SECOND ORDER RECONFIGURABLE LOWPASS FILTER

2.1 Overview of the source follower based filter

The second order low pass filter having source follower architecture is proposed for the first time in [12]. This architecture has the following advantages:

(1) It results in low output impedance and a resistive load can be driven with negligible effects on the filter performance in terms of linearity and filter transfer function accuracy.

(2) The inherent feedback present in the structure gives better linearity.

(3) Distortion introduced in the voltage to current conversion process in the case of current mode filters does not arise.

In order to enable tunability and to eliminate bottom plate capacitance, filter proposed in [11] is modified and is shown in Fig.1. It has a fully differential structure and operates like a "composite" source-follower. It provides an ideal unity DC-gain. All the transistors are designed to be of the same size and draw the same current. As a result, they all exhibit the same transconductance values. Assuming that the transistor's output conductance (g_{ds}) is much smaller than the transconductance (g_m), the filter transfer function can be shown [11] to be that given in (1)

$$H(S) = \frac{1}{S^2.\frac{C_1C_2}{g_m^2} + S.\frac{C_1}{g_m} + 1} \tag{1}$$

where g_m is the transconductance of the transistor, C_1 and C_2 are the capacitors.

The filter parameters (the pole frequency, the quality factor, and the DC-gain) are given by

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{2}$$

$$\omega_0 = 2.\pi.f_0 = \frac{g_m}{\sqrt{C_1C_2}} \tag{3}$$

From (3), it is clear that by varying the g_m and the capacitor values, we can vary the frequency of operation.

2.2 Reconfigurable lowpass filter in subthreshold region

The modification of the low pass filter shown in Fig. 1, for the bandwidth to be programmable from 100KHz to 20MHz is considered next. Let us assume that a butterworth filter with quality factor of 0.707 and capacitors C_1 and C_2 of values 0.5pF and 1pF respectively are used for the filter. For this filter, the g_m required for this frequency range varies from 1.3µS – 206µS. This g_m value, is obtained by operating the transistor of source follower circuit in weak inversion/subthreshold region.

The operation of the filter in weak inversion mode is quite suited for low power and low frequency applications because of the following reasons:

1) The maximum voltage swings between the terminals of the devices working in the weak inversion region are smaller than those working in strong inversion region. This permits the use of lower supply voltages and there by reduces the power consumption.

2) Low pass filters require smaller transconductance (g_m) and larger capacitance (C_{GS} and C_{GD}). The value of these capacitances may be increased by increasing the product of width (W) and length (L) of the device. However, in order to obtain lower g_m, the width has to be small. Hence, the length of the device is increased. Use of devices with larger length results in better matching of devices.

3) The output common mode voltage is self biased by the transistor V_{GS}. This relaxes the need for CMFB (common mode feedback) circuit which in turn reduces the power dissipation.

The transconductance (g_m) of the transistor operating in the subthreshold region is given by (4)

$$g_m = \frac{I_D}{\mathbf{n\Phi_T}} \tag{4}$$

where 'n' is sub threshold slope factor (1.5) and 'Φ_T' is thermal voltage (25.9 mV @ room temperature). I_D is the current of a MOS transistor [12] and is given by (5),

$$I_D = 2.n.k.\Phi_T^2.\exp\left(\frac{V_{GB} - V_{T0}}{n.\Phi_T}\right) * \left[\exp\left(\frac{-V_{SB}}{\Phi_T}\right) - \exp\left(\frac{-V_{DB}}{\Phi_T}\right)\right] \tag{5}$$

where 'µ' is mobility, 'C_{ox}' is the oxide capacitance of the transistor, $\beta = \mu.C_{ox}$ is the process gain factor and transconductance parameter $k = \beta.(W/L)$, V_{GB}, V_{SB}, V_{DB} are gate, source, drain voltages w.r.t. bulk respectively, V_{T0} is the threshold voltage when V_{SB} is zero.

For operation in subthreshold region, $V_{DB} > 5\ \Phi_T$ and $V_{SB} = 0$. In this case, (5) simplifies to that given in (6).

$$I_D = 2.n.k.\Phi_T^2.\exp\left(\frac{V_{GS} - V_{T0}}{n.\Phi_T}\right) \tag{6}$$

From (4), it can be noted that for the required g_m range, the current is to be varied between 32nA to 8.2µA. Using (6) and assuming V_{T0} of 0.5V and W/L of the transistor to be 80µm /0.5 µm, V_{GS} can be found to be 220mV to 440mV. The supply voltage used is 1.2V. This requires the DAC voltage to be varied in the range 760mV – 980mV. The length of the transistors used for the above filter is chosen taking into account quality factor (Q) and linearity. The sensitivity of the Q factor with respect to the output MOS conductance, g_{ds} , can be shown [12] to be that given in (7)

$$S_{g_{ds}}^{Q} = \frac{\partial Q}{\partial g_{ds}}.\frac{g_{ds}}{Q} \approx -\frac{3}{2}\frac{g_{ds}}{g_m} \tag{7}$$

In order to make the Q factor to be independent of variations in output conductance (g_{ds}), g_{ds} has to be chosen to be small. Next, let us consider the effect of length of the transistor on the linearity of the filter.

As the filter structure is fully differential, second order harmonic HD2, gets cancelled out. Assuming that the third

harmonic distortion (HD3) is the main contribution to the total harmonic distortion, when transistors operate in weak inversion, the HD3 can be shown to be that given in (8) at low frequencies.

$$\mathbf{HD3} = \frac{1}{6}.\frac{v_{\mathbf{in}}^2}{\left(n.\frac{\mathbf{kT}}{q}\right)^2}.\frac{1}{\left(1+\frac{g_m}{g_{\mathbf{d0}}}\right)^2} \approx \frac{1}{6}.\frac{v_{\mathbf{in}}^2}{\frac{1}{\lambda^2}} \tag{8}$$

From (8), it may be noted that the linearity can be increased by increasing λ (channel length modulation coefficient). This in turn requires the length of the transistors to be increased. To have low g_{ds} value and high linearity, the length of the transistor is chosen to be 0.5µm for our implementation in 0.18µm CMOS technology.

2.3 Noise Performance of the proposed filter

At very low frequencies corresponding to the biomedical signals, only the flicker noise component of the transistors is dominant. In order to reduce the flicker noise, PMOS transistors are preferred. The flicker noise is inversely proportional to gate area (WxL). In order to reduce this noise, the gate area should be increased. However, since the proposed filter requires lower transconductance of the order of nS, the W/L ratio required is low and hence transistors with larger length and smaller widths are chosen.

The input referred voltage noise of the second order source follower circuit may be calculated using the half circuit noise model shown in Fig. 2. Let the mean square noise voltages corresponding to the transistors M4, M2 and M0 be denoted as V_{n1}^2 , $V_{\mathbf{n2}}^2$ and $V_{\mathbf{n3}}^2$ respectively. It may be noted that the dimensions of all these transistors are the same. The mean square input-referred voltage noise (V_n^2) due to the flicker noise of a transistor[13] is given by

$$V_n^2 \approx \frac{K_f}{c_{\mathbf{ox}}^2.W.L.f} \tag{9}$$

where C_{ox} is the oxide capacitance, f is the frequency, K_f is the flicker noise coefficient . It varies between 10^{-22} to 10^{-24}. The mean square input referred noise voltage of the second order source follower circuit using the half circuit model can be shown to that given in (10)

$$v_{\mathbf{in,n}}^2 \approx \frac{6.k_f g_m^2}{c_{ox}^2.f.W.L}\left\{\frac{r_{o2}\left(g_m + (r_{o2} \,||\, r_{o1})^{-1}\right)}{g_m}\right\} \tag{10}$$

where r_{o1} and r_{o2} are the output resistance of the transistors M1 and, M2 respectively. As the gain of the circuit is unity, both the output referred noise and the input referred noise are same. Using (8), for a given HD3, the value of $V_{\mathbf{in,rms}}^2$ can be found out. Using this in (10), the dynamic range is estimated and is given by (11)

$$\mathbf{DR} = \mathbf{10}.\log_{\mathbf{10}}\left(\frac{V_{\mathbf{in,rms}}^2}{V_{\mathbf{in,n}}^2}\right) \tag{11}$$

2.4 Minimum supply voltage required for the filter

Since the design proposed is targeted for low power application, the supply voltage should be as small as possible. In this paper, for the implementation of the filter in 0.18µm CMOS technology, V_t of 0.5V, maximum V_{gs} of 450mV and voltage swing of 200mV are assumed. This makes the V_{sat} of PMOS transistors to be 50mV and it ensures the transistors to be in weak inversion region. Using these voltages, the minimum supply voltage required for the PMOS source follower filter shown in Fig. 2 is given by (12).

$$V_{\mathbf{dd,min}} \geq \mathbf{3v_{sat}} + v_t + v_{\mathbf{swing}} \tag{12}$$

From (12), it may be verified that $V_{dd,\,min}$ should be at least 0.9V. For our design, a supply voltage of 1.2V is chosen.

3. DAC DESIGN

In this paper, a 7 bit current steering DAC is used to produce necessary bias voltages V_{bias} required for frequency tuning. The circuit diagram of the proposed DAC is shown in Fig. 3. As mentioned in section 2.3, the bias voltage required to tune the filter from 100KHz – 20MHz is 980mV – 760mV. The supply voltage to the DAC is 1.2V. To obtain 980mV, the switch corresponding to the most significant bit "b7" is always tied to 1.2V. The load resistor of DAC is fixed at 500 ohms. The full scale voltage range of the DAC is 220mV. The voltage resolution of least significant bit is 3.43mV. The W/L ratio of the current source transistor corresponding to bit "b0" is calculated as 0.25µm /1µm.

The successive bits b1 – b7 are scaled accordingly. The dimensions of the switches are the same as that of respective current source transistors. When the bits b1- b6 are all high, the DAC produces 760mV, making the filter to exhibit a cutoff frequency of 20MHz. Similarly, if all bits b1- b6 are low, DAC produces 980mV, making the filter to exhibit a cutoff frequency of 100KHz.

4. SIMULATION RESULTS

The reconfigurable Gm-C lowpass filter is implemented in TSMC 0.18µm CMOS technology with 1.2 V supply voltage. From simulation, it is estimated that the lowpass filter block consumes power of 1µW at 100 KHz and 20µW at 20 MHz.

The coarse tunability of the centre frequency of the filter for various DAC voltages are shown in Fig 4. From these results it may be noted that the bandwidth can be tuned from 100 kHz to 20 MHz achieving a tuning range of more than two orders of magnitude. This bandwidth range meets almost all wireless applications (GSM, Bluetooth, CDMA2000, W-CDMA/UMTS and WLAN a/b/g receivers with zero IF). The 7 – bit CSDAC output voltage for counter input is shown in Fig 5. It demonstrates that it can provide bias voltages in steps of 3.4mV from 980mV – 760mV. Finer resolution of tuning range is possible by increasing

the resolution of the DAC. The power consumption of the DAC is 865µW.

Fig. 6 shows an IIP3 (Third order Input Intercept Point) measurement using two in-band tones that are close in frequency with f_0=10MHz. An IIP3 of 15 dBVp is achieved. Repeating this test near f_0 =20MHz, the IIP3 drops to 7 dBVp and is shown in Fig. 7. The SFDR plot for peak to peak input voltage of 300mV w.r.t 20MHz input is shown in Fig. 8. It can be noted from this figure that the upper bound on THD is -40dB (1%) for 300mVpp signal swing. Fig .9 shows the equivalent input referred noise of the filter. The total input referred integrated noise is computed to be 55µVrms. This yields 66 dB dynamic range.

The simulation results of the proposed design are compared with other filter realizations and are reported in Table 1. The proposed filter consumes 14 times less power than that of [10] without any compromise on other parameters. The input referred noise of the source follower filter is 1.5 times higher than that of [10] is due to the fact that the gain of the source follower architecture is lesser than the former.

5. CONCLUSIONS

A reconfigurable continuous time low pass filter based on source follower is implemented in TSMC 0.18 µm digital CMOS process. Due to the subthreshold operation of the filter more than two fold reduction in power is achieved than that of [10]. The designed low pass filter features a good center frequency tuning from 100KHz to 20MHz which covers the frequency range corresponding to analog baseband filters used in the physical layer of various wireless networks such as WLAN a/b/g , UMTS, Bluetooth, GSM and CDMA. Since the analog baseband circuit not only requires lower area and power, but also has a good reconfigurablity, it is a strong candidate for utilization as one of the building blocks for SDR transceivers.

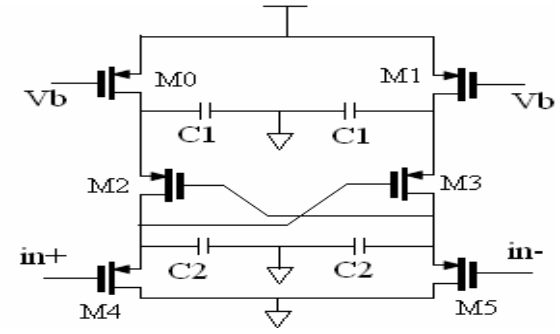

Fig. 1. Second order source follower filter

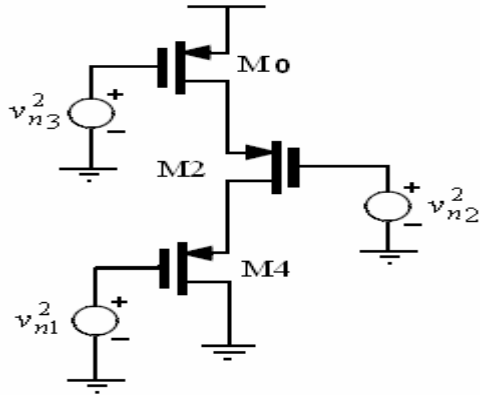

Fig. 2. Half circuit noise model for source follower filter

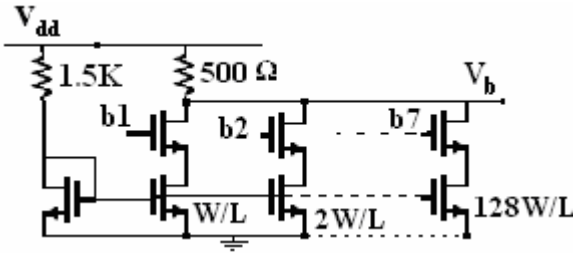

Fig. 3. Seven bit CSDAC

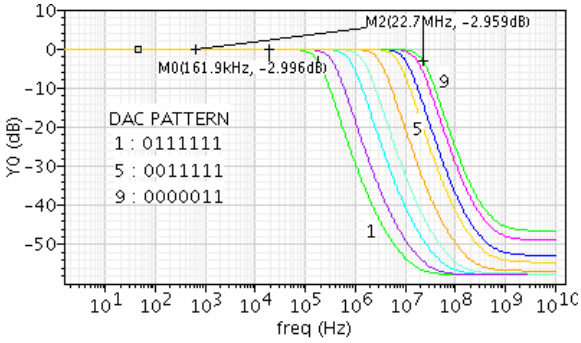

Fig. 4. Magnitude response of the filter for various DAC settings

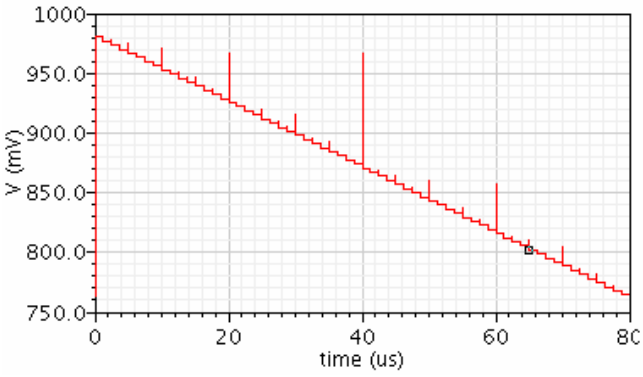

Fig. 5. Output voltage of CSDAC for counter input.

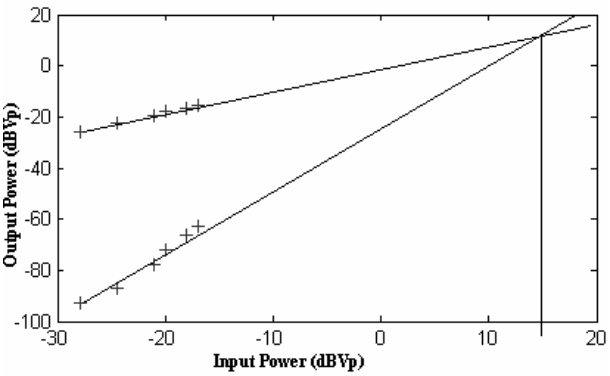

Fig. 6 . IIP3 plot for in band tones (f_0= 10MHz)

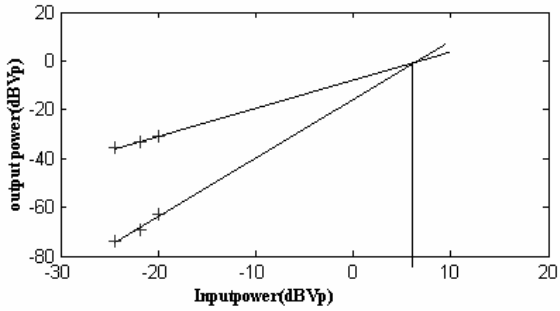

Fig. 7. IIP3 plot for in band tones (f_0= 20MHz)

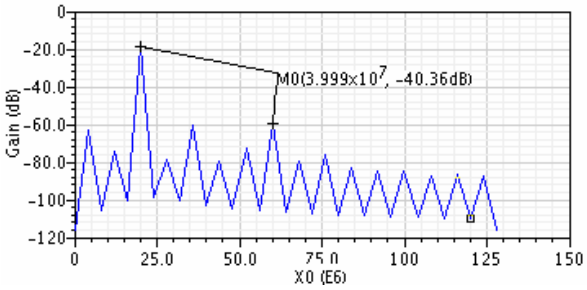

Fig. 8. SFDR plot for 300mVpp, 20MHz input.

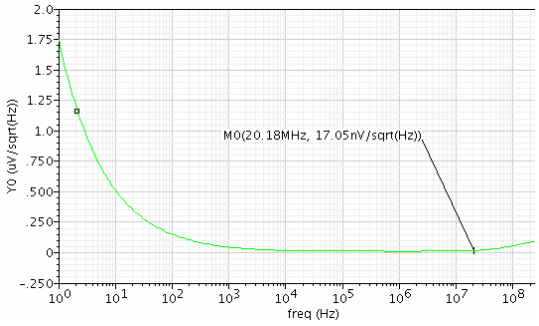

Fig. 9. Input referred noise of the filter

Table 1. Performance summary

Parameters	**[10]**	**This work**
Technology	0.13µm CMOS	0.18µm CMOS
Filter	2nd order Butterworth	2nd order Butterworth
Supply voltage	1.2V	1.2V
IIP3	10dBVp @10MHz	15dBVp @10MHz
Input referred noise	36µVrms	55 µVrms
BW (Programm-able)	100KHz to 20MHz	100KHz to 20MHz
Tuning range	200	>200
Active area	0.5mm^2	--
Power	14.2mW	0.95mW
Vinpp @ THD=-40dB	200mV	300mV
DR@ THD≤-40dB	68dB	66dB

REFERENCES

[1] V. Giannini, J. Craninckx, A. Baschirotto,"Baseband Analog circuits for Software Defined Radio", *Springer, New York,* 2008, chapter 5.

[2] M. Laugeois, "Reconfigurability Approach on Hardware Design for MTS Terminal", *MUMOR Project, Lausanne,* 2004.

[3] Workshop on Multi-Mode Multi-Band Re-Configurable Systems for 3rd Enhanced Generation Mobile Phones, *MUMOR Project Leuven, Belgium,* 2004.

[4] S.D'Amico *et al*., "Low-power reconfigurable baseband block for UMTS/WLAN transmitters", *Proc. Of NORCHIP,* pp. 103-106,November 2004.

[5] Stefano D'Amico, Vito Giannini, and Andrea Baschirotto, "A 4th-Order Active-Gm-*RC* Reconfigurable (UMTS/WLAN) Filter", *IEEE J.Solid- State Circuits*, vol. 41, pp. 1630– 1637, July 2006.

[6] V.Giannini, J. Craninckx, J. Compiet, B. Come, S. D'Amico,A.Baschirotto,"Flexible baseband Low-Pass Filter and Variable Gain Amplifier for Software Defined Radio Front End", *Proc. Of ESSCIRC*2006, pp. 203-206, September 2006.

[7] D. Chamla, A. Kaiser, A. Cathelin, and D. Belot, "A Gm-C low-pass filter for zero-IF mobile applications with a very wide tuning range", *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1443–1450, Jul. 2005.

[8] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies", *IEEE J. Solid-State Circuits*, vol. 27, pp.142–153, Feb.1992.

[9] F. Munoz, A. Torralba, R. G. Carvajal, and J. Ramirez-Angulo, "Two new VHF tunable CMOS low-voltage linear transconductors and their application to HF gm-C filter design", in *Proc. ISCAS,* May 2000, pp.V-173–176.

[10] P. Crombez, J. Craninckx, Piet Wambacq and M. Steyaert, "A 100-KHz to 20-MHz Reconfigurable Power-Linearity Optimized Gm–C Biquad in 0.13❍m CMOS", *IEEE Transactions on Circuits and Systems* II: Express Briefs, vol. 55, Mar 2008, 33, pp.224- 228.

[11] S. D'Amico, Matteo Conta, and Andrea Baschirotto, "A 4.1-mW 10-MHz Fourth-Order Source- Follower-Based Continuous-Time Filter with 79-dB DR", IEEE JSSC, vol.41,no 12,pp. 2713-2718, Dec 2006.