High Performance of Sinusoidal Pulse Width Modulation Based Flying Capacitor Multilevel Inverter fed induction Motor Drive

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ABSTRACT
This paper focused on the development of capacitor voltage balancing methods in a flying capacitor multilevel inverter (FCMLI) fed induction motor drive. For improving the performance of flying capacitor multilevel inverter, a switching pattern selection scheme is implemented. The proposed method has been designed a seven-level flying capacitor multilevel inverter by using sinusoidal pulse width modulation technique. The selected pattern has been exposed to give superior performance in load voltage, total harmonics distortion and capacitor voltage fluctuation. The performance of proposed strategies is confirmed through simulation investigations.

Keywords
AC Drive, Flying Capacitor Multilevel Inverter (FCMLI), Total Harmonic Distortion, Sinusoidal pulse width modulation (SPWM).

1. INTRODUCTION
In recent year, multilevel power inverters are popular due to their high-power, high voltage capacity, low switching losses and low cost. The various different topologies of inverters are neutral point clamped inverters, flying capacitor inverters and cascaded multi level with separated dc source inverter [1]-[2]. Midway the Flying Capacitor Multi-level Inverter (FCMI) does not require isolated dc sides and additional clamping diodes. However, these properties may be quite limited by the voltage unbalancing of flying capacitors which the most serious problem.

Hence the FCMLI has to ensure the voltage balancing of flying capacitors under all the operating conditions. The FCMLI offers a great advantage with respect to the availability of voltage redundancies. They are defined as different combinations of capacitors allowing the charging or discharging of the individual flying capacitors in order to produce the same phase leg voltage. This advantage provides the special opportunity for controlling

the individual voltage on flying capacitors [3]-[4]. Many studies have publicized that under certain conditions, a simple open loop control guarantees natural balancing of the flying capacitor.

A filter circuit of the *RLC* type tuned at the switching frequency, connected in parallel with the load may be used to achieve the natural balancing under all conditions. However, the extra filter

increases the cost of the overall system. Another popular method of capacitor voltage balancing is to vary duty cycles of the switches to charge or discharge the corresponding capacitors. There are many ways such as carrier rotation strategy [5]-[7], modulating signal modification strategy [8], etc. In the control scheme discussed in [9]-[10], balancing is achieved by preferential charging or discharging of the capacitors.

This paper highlights the sinusoidal pulse width modulation technique. This scheme does not require any modification in the carrier or modulating signal.

2. FLYING CAPACITOR MULTILEVEL INVERTER (FCMLI)
The FCMLI requires a large number of capacitors to clamp the device voltage to one capacitor voltage level, provided all the capacitors are equal values. The size of the voltage increases between two consecutive legs of the clamping capacitors. Hence the size of voltage steps in the output waveform.

2.1 Basic Configuration of FCMLI
The voltage of the main dc-link capacitor $V_{dc.}$ The voltage of the capacitor clamping of the innermost two devices are

$$\frac{V_{dc}}{n-1} \quad (1)$$

.

The voltage of the next innermost capacitor will be

$$\frac{V_{dc}}{n-1}+\frac{V_{dc}}{n-1}=\frac{2V_{dc}}{n-1} \quad (2)$$

Each next clamping capacitor will have the voltage increment of $\frac{V_{dc}}{n-1}$ from its immediate inner one. The voltage levels and the arrangements of the flying capacitor in the FCMLI structure assure the voltage stress across each main device is same. It is equal to $\frac{V_{dc}}{n-1}$ for an n- level inverter.

Three phase of a seven-level inverter fed induction motor as shown in figure 1. Three out of one phase leg of a seven-level inverter shown in figure 2 and likewise others two are coupled to

the same dc-link battery V_{dc}. In figure 1 each switch S_{A1} to S_{A6} and S'_{A1} to S'_{A6} consist of a power semiconductor device (e.g. MOSFET, GTO and IGBT etc) connected in anti-parallel. The capacitor voltages are, V_c, V_{c2} to V_{c6} and V_{dc}, $\frac{5}{6}V_c$ to $\frac{1}{6}V_{dc}$ respectively, as $n = 7$.

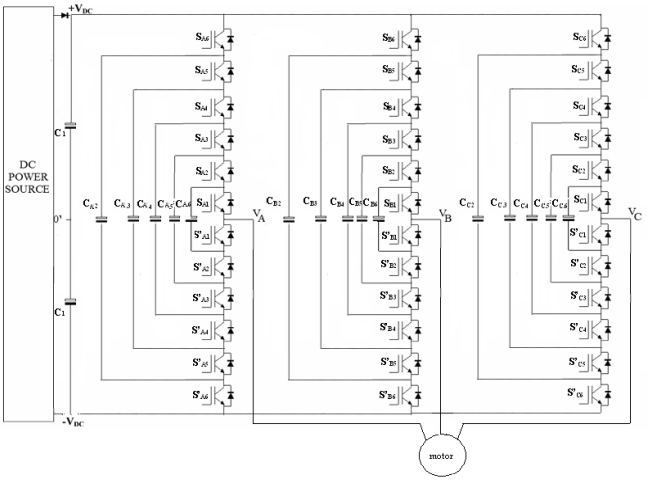


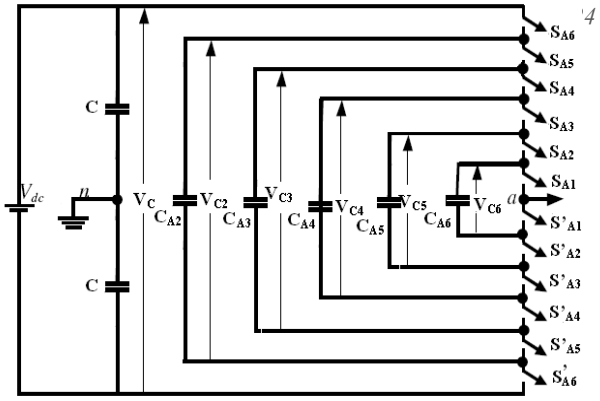
Figure 1. Seven level inverter fed three phase Induction motor.

The switch combinations given in Table I are used to synthesize the output voltage of phase-A, V_{an}, with respect to the neutral point *n*. The main dc capacitor combination C is the energy storage element, while capacitors C_{A2}, C_{A3}, C_{A4}, C_{A5} and C_{A6} are the flying capacitors that provide the multilevel voltage ability to the converter. The pair of switches (S_{A1}, S'_{A1}), (S_{A2}, S'_{A2}), (S_{A3}, S'_{A3}), (S_{A4}, S'_{A4}), (S_{A5}, S'_{A5}) and (S_{A6}, S'_{A6}) are connected in complementary nature.

Thus if S_{A1} is ON, S'_{A1} is OFF and vice-versa. For any initial state of clamping voltage, the inverter output voltage is given by

$$V_{an} = S_{A1}(V_c - V_{c2}) + S_{A2}(V_{c2} - V_{c3}) + S_{A3}(V_{c3} - V_{c4}) + S_{A4}(V_{c4} - V_{c5}) + S_{A5}(V_{c5} - V_{c6}) + S_{A6}V_{c6} - \frac{V_c}{2} \quad (3)$$

Figure 2. Phase-A leg of the seven level inverter.



2.2 Modulation Scheme

In the paper control technique of sinusoidal pulse width modulation (SPWM) strategy is employed. In this method, a number of triangular waveforms are compared with a controlled sinusoidal modulating signal. The switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal [8, 9, and 10]. The proposed seven level inverter, one modulating signal and six carrier waves are necessary for each phase of the inverter as shown in Figure 3.

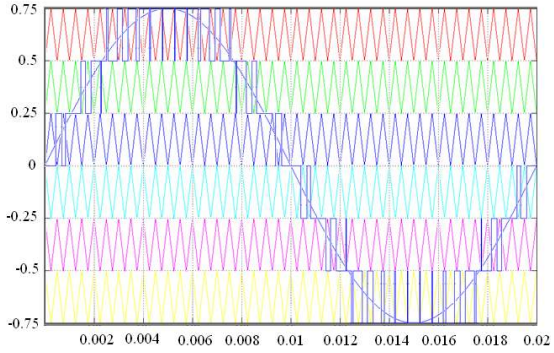


Figure 3. Modulation scheme for seven level .

The modulating signal of each phase is displaced from each other by 120°. All the carrier signals have same frequency *fc* and amplitude *Ac* while the modulating signal has a frequency of *fm* and amplitude of *Am*.

The *fc* should be in the multiples of *fm* with three-times. This is required for all the modulating signal of all the three phases see the same carriers, as they are 120° apart.

The output voltage is obtained, by comparing the carrier voltage signal and the modulating voltage signal. The modulating signal varies from + 1.5V to – 1.5V. The six carrier waves are +ve and – ve half cycles have the amplitude varying from 0 to 0.25, 0.25 to 0.5, 0.5 to 0.75, and 0 to – 0.25, and -0.25 to – 0.5,-0.5 to -0.75 respectively. In the positive half cycle the output will have the value + 0.5 if the amplitude of the modulating signal is greater than that of the carrier wave (0 to 0.25) and 0 otherwise.

Similarly for the negative half cycle if the modulating signal is lower than the carrier wave (0 to –0.25), the output of the comparator is – 0.5 and 0 otherwise. If the modulating signal is greater than two carrier waves in the positive and negative half cycle,Then the output is +1. If the modulating signal is greater than three carrier waves in the positive half, the output is + 1.5. Likewise negative half cycle. In this way 7 output levels (+1.5, +1, 0.5, 0,-0.5,-1,-1.5) are obtained. The SPWM output reference signal is shown in Figure 3. This signal resembles with the output voltage waveform of the inverter and decides the voltage level, which is to be generated at a particular instant.

Table I. Switching scheme for phase-A leg.

S_{A6}	S_{A5}	S_{A4}	S_{A3}	S_{A2}	S_{A1}	C_{A2}	C_{A3}	C_{A4}	C_{A5}	C_{A6}	V_{an}
ON	ON	ON	ON	ON	ON	NC	NC	NC	NC	NC	$V_{dc}/2$
ON	ON	ON	ON	ON	OFF	NC	NC	NC	NC	+	$V_{dc}/3$
ON	ON	ON	ON	OFF	ON	NC	NC	NC	+	-	
ON	ON	ON	OFF	ON	ON	NC	NC	+	-	NC	
ON	ON	OFF	ON	ON	ON	NC	+	-	NC	NC	
ON	OFF	ON	ON	ON	ON	+	-	NC	NC	NC	
OFF	ON	ON	ON	ON	ON	-	NC	NC	NC	NC	
OFF	OFF	ON	ON	ON	ON	NC	-	NC	NC	NC	$V_{dc}/6$
OFF	ON	OFF	ON	ON	ON	-	+	-	NC	NC	
OFF	ON	ON	OFF	ON	ON	-	NC	+	-	NC	
OFF	ON	ON	ON	OFF	ON	-	NC	NC	+	-	
OFF	ON	ON	ON	ON	OFF	-	NC	NC	NC	+	
OFF	ON	ON	ON	OFF	OFF	-	NC	NC	+	NC	0
OFF	OFF	ON	ON	ON	OFF	NC	-	NC	NC	+	
OFF	OFF	OFF	ON	ON	ON	NC	NC	-	NC	NC	
ON	OFF	OFF	OFF	ON	ON	+	NC	NC	-	NC	
ON	ON	ON	OFF	OFF	OFF	NC	NC	+	NC	NC	
ON	OFF	OFF	OFF	OFF	ON	+	NC	NC	NC	-	$-V_{dc}/6$
ON	OFF	OFF	OFF	ON	OFF	+	NC	NC	-	+	
ON	OFF	OFF	ON	OFF	OFF	+	NC	-	+	NC	
ON	OFF	ON	OFF	OFF	OFF	+	-	+	NC	NC	
ON	ON	OFF	OFF	OFF	OFF	NC	+	NC	NC	NC	
ON	OFF	OFF	OFF	OFF	OFF	+	NC	NC	NC	NC	$-V_{dc}/3$
OFF	ON	OFF	OFF	OFF	OFF	-	+	NC	NC	NC	
OFF	OFF	ON	OFF	OFF	OFF	NC	-	+	NC	NC	
OFF	OFF	OFF	ON	OFF	OFF	NC	NC	-	+	NC	
OFF	OFF	OFF	OFF	ON	OFF	NC	NC	NC	-	+	
OFF	OFF	OFF	OFF	OFF	ON	NC	NC	NC	NC	-	
OFF	OFF	OFF	OFF	OFF	OFF	NC	NC	NC	NC	NC	$-V_{dc}/2$

In Table I, NC indicates that there is no change in the state of the corresponding capacitor, i.e., the capacitor neither charges nor discharges. The states + ve and − ve denote the charging and discharging of the capacitors.

3. FEATURES OF FCMLI

- Voltage stresses across the devices are equal.
- Reduce the redundancy of switching combinations.
- Only single capacitor voltage regulating circuit is required.

4. PROJECTED METHOD

In the projected method, seven levels inverter is designed. The output voltages nearly get sinusoidal. Hence reduced harmonics and increase inverter efficiency. Some soft switching method can be used for multilevel inverters to reduce the switching loss. The seven level flying capacitor inverter fed induction motor drive has been developed by using MATLAB software.

5. RESULT ANALYSIS

The seven-level FCMLI has been simulated by using MATLAB. The output of the inverter voltage is shown in simulation results. Chapter 5.1 deals with Seven-Level Flying capacitor multilevel inverter output voltages. Chapter 5.2 deals with multi level inverter fed induction motor and analysis its performance like speed, electromagnetic torque and stator current.

5.1 Seven-Level FCMLI Simulation Results

The FCMLI output balanced three phase voltage is 200Volts with seven levels as shown in figure 4.The line voltage is about 400V as shown in figure 5 and final obtained three phase output voltage with minimum harmonics shown in figure 6. The inverter output is given to a balanced three-phase induction motor. The inverter parameters are given in Table II.

Table. II Seven-level Inverter parameters

Number of main switches	36
Main devices type	IGBT
Device ON resistance	0.01 ohm
Device OFF resistance	1.0E6 ohm
Forward voltage drop	0 V
FCMLI capacitances	3600 µF

The seven levels of three phase voltages are ($\pm\frac{V_{dc}}{2}$, $\pm\frac{V_{dc}}{3}$, 0, $\pm\frac{V_{dc}}{6}$).The line to line voltages have fourteen levels.

Figure 4. Phase voltage of FCMLI

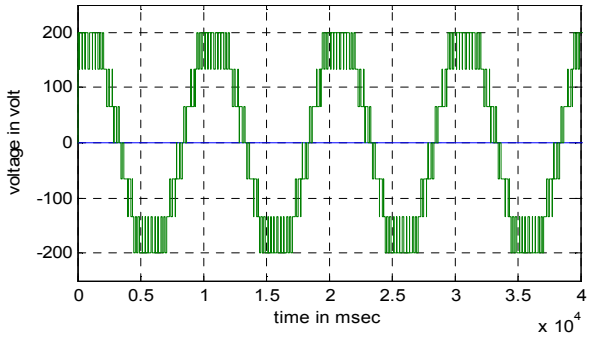
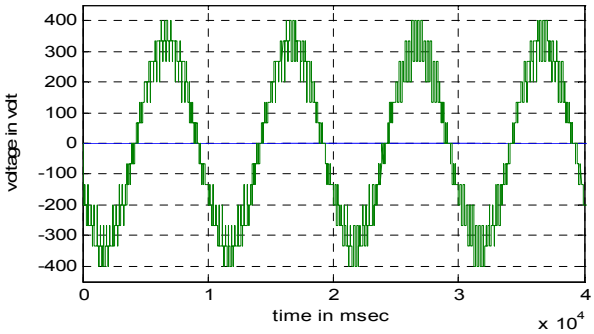


Figure 5. Line voltage of FCMLI



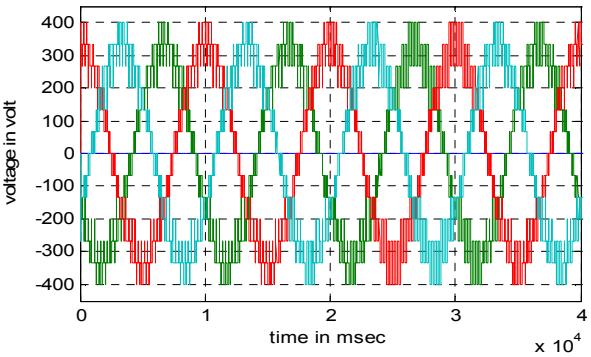


Figure 6. Three phase output line voltage of FCMLI

The capacitor balanced charging and discharging of leg voltages V_{C2}, V_{C3} V_{C4}, V_{C5}, and V_{C6} as shown in Figure 7. The voltage across each individual capacitor is $V_{dc}/3$. The fluctuation in capacitor voltage is tiny. This can be further reduced by increasing capacitance values and carrier frequency.

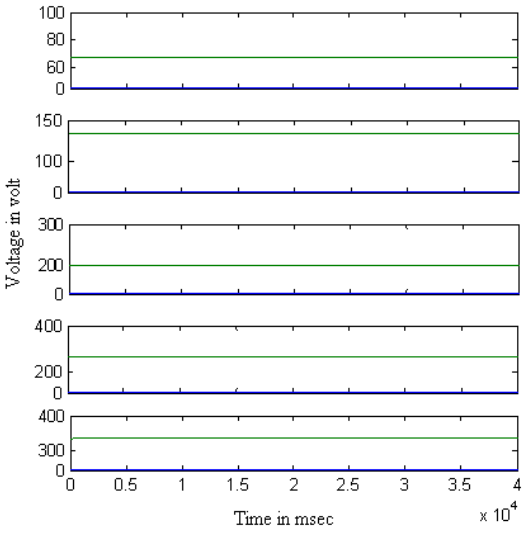


Figure 7.Capacitor leg voltages of V_{C2} to V_{C6}

5.2 Seven-Level FCMLI fed Induction Motor

Induction motors are widely used in industries because it offers lot of advantages. The proposed method of a seven-level FCMLI is fed to induction motor drive of rating 5HP, 400V and supply frequency of 50Hz, speed of 1500rpm. A seven level FCMLI fed induction motor speed curve result shown in figure 8. It quickly settle to a constant speed of 1500rpm.The electromagnetic torque of induction motor as shown in figure 9 and figure 10 illustrated in stator current. Initially it has maximum starting current then get reduced at rated value of the motor current.

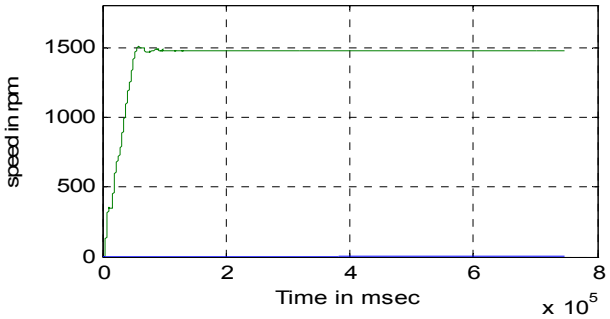


Figure.8 Speed curve of induction motor

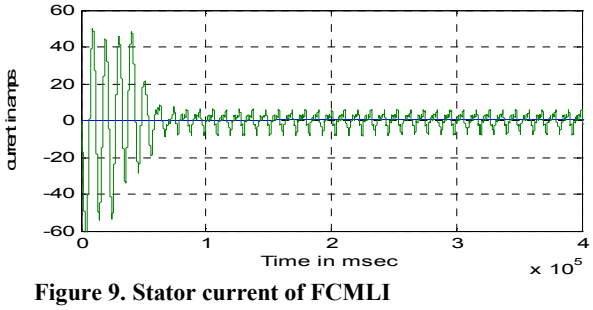


Figure 9. Stator current of FCMLI

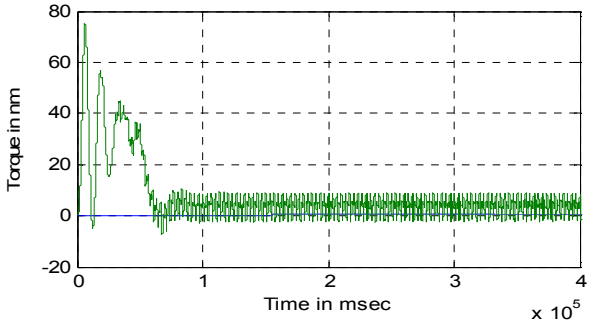


Figure.10 Torque curve of induction motor.

Total Harmonic Distortion of seven level FLCMLI is 17.75% which is illustrated in figure 11. In seven level inverter total harmonic distortions was reduced when compare to five level FCMLI. It is increased to nine and eleven level inverter, THD are reduced to 13.34%, 10.62% respectively.

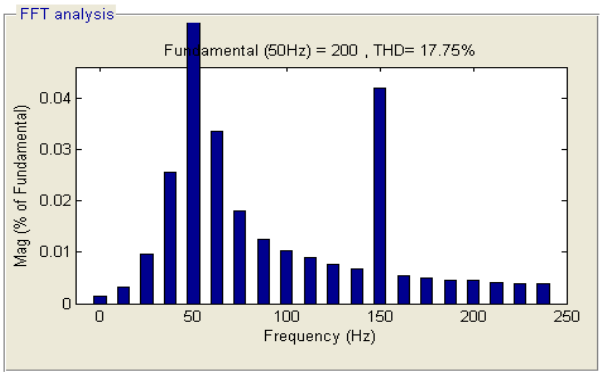


Figure.11 THD of seven levels FCMLI.

6. CONCLUSION

In the proposed method, seven levels flying capacitor multilevel inverter provides sinusoidal waveform and increased efficiency. The basic concepts and operational features of inverter have been explored. A control scheme has been proposed which uses the preferential charging or discharging of flying the capacitors to balance their voltages. The control scheme allows balanced flying capacitor voltages; hence output phase and line voltages are obtained with much less THD. The seven level flying capacitor multilevel inverter fed induction motor has been illustrated with simulation results using MATLAB. The technique is used to improve the level of the inverter to extend the design flexibility and reduces the harmonics.

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